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VOL. 10 No. 92 MARCH 1968

N.G.W.

Mullard Technical Communications

VOLUME 10 NUMBER 92

March 1968

Mullard

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All articles in *Mullard Technical Communications* are indexed in *British Technology Index*. Abstracts appear in *Current Papers in Physics, Electrotechnology, and Control.*

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Editor: F. A. Sowan
Assistant Editors: E. G. Evans A. Perry

Published by
Central Technical Services
Mullard Limited, Mullard House, Torrington Place, London, W.C.1
Telephone: 01-580 6633 Telex: 264341

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Made and Printed in England by
WIGHTMAN AND COMPANY LIMITED, 1/3 BRIXTON ROAD, LONDON, S.W.9

Voltage Regulation of Lower-powered Alternators

J. Lavallee
Mullard Central Application Laboratory

A system for the regulation of the output voltage of an alternator by field current control is described. The control of the field current is achieved by a single thyristor used in conjunction with a novel a.c. feedback system; the a.c. output from the alternator is used for voltage sensing. This eliminates the need for a transformer and rectifier sensing unit at the output of the alternator. The voltage control unit has dimensions comparable to thyristor trigger modules.

The voltage regulation obtained from a 50Hz alternator with a complex load was within 1%, and was also within 5% with a transient overload of 50%. A 400Hz alternator was well within 1% regulation on a 50% overload.

INTRODUCTION

Small petrol or diesel driven alternator sets have catered for two quite separate markets. Firstly, on sites where mains supply is not readily available and where good voltage regulation is not of prime importance; internal self-compensation is all that is necessary. Secondly, on more sophisticated installations where the alternator acts as a stand-by supply for a telecommunications link, or on aircraft ground installations demanding more stringent specifications; here automatic voltage regulation is desirable to maintain a constant output when a variable load is applied.

This article describes how thyristors can be used to control the output by varying the current through the field windings of a single-phase or a three-phase alternator, (see Fig. 1).

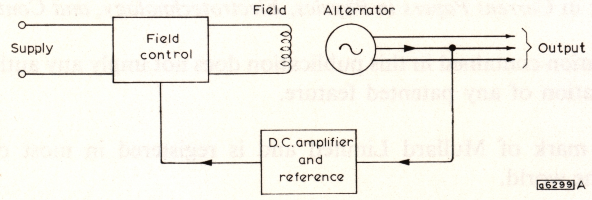
Supply
Field control
Field
Alternator
Output
D.C. amplifier and reference

Fig. 1—Automatic voltage regulator

The circuit described in this article uses a novel method of control* which has the advantage of using the raw a.c. supply from the alternator for its voltage sensing. This eliminates the need for a transformer and rectifier sensing unit on the input. The sensing signal does not require smoothing so the system 'time lag' is greatly reduced (to 3 cycles in 50) and system stability is considerably improved.

The voltage regulation obtained from a 50Hz alternator with a complex load was within 1%, and was also within 5% with a transient overload of 50%. A 400Hz alternator was well within 1% regulation on a 50% overload.

METHODS OF REGULATION

Voltage regulation of alternators has in the past been provided by complex and sometimes bulky circuits.

Carbon Pile

Carbon pile control of field current (Fig. 2) is seldom used in modern alternators because it has a slow response, good regulation cannot easily be obtained, it is difficult to set up, and requires frequent maintenance.

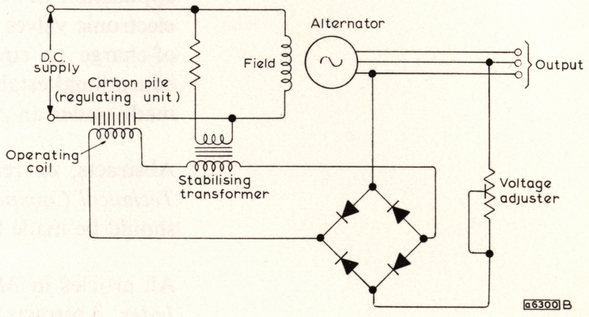
D.C. supply
Carbon pile (regulating unit)
Operating coil
Field
Alternator
Output
Stabilising transformer
Voltage adjuster

Fig. 2—Carbon pile regulator

Saturable Reactor

The saturable reactor or transductor (Fig. 3) with a magnetic amplifier is mainly used to obtain good regulation from high-powered alternators above 100kVA, but it has a slow response. It also requires many large components, which make this system expensive.

D.C. Chopper

The d.c. chopper method (Fig. 4), using thyristors, offers a wide range of power control combined with fast response. Many different types of d.c. chopper could be used, and would give little waveform distortion when using high chopper frequencies.

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*British Patent applied for.

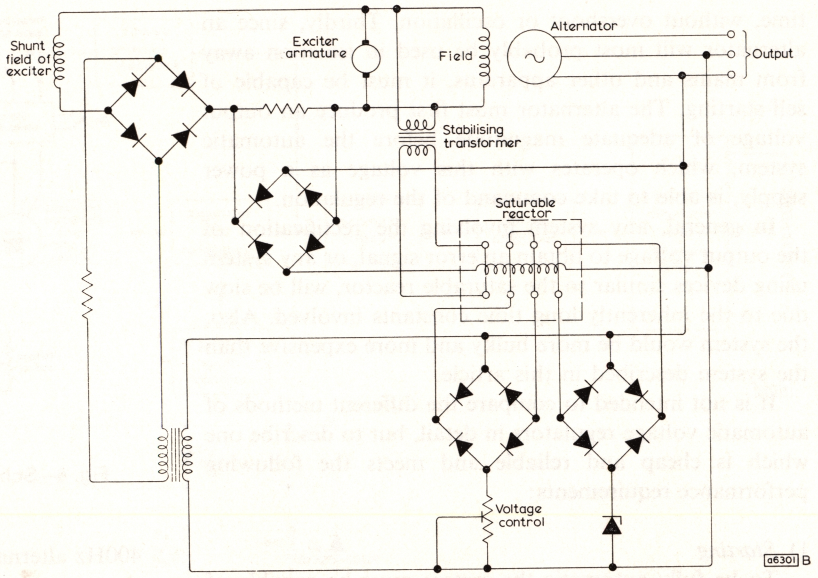

Shunt field of exciter
Exciter armature
Field
Alternator
Output
Stabilising transformer
Saturable reactor
Voltage control

Fig. 3—Simple circuit of saturable reactor regulator

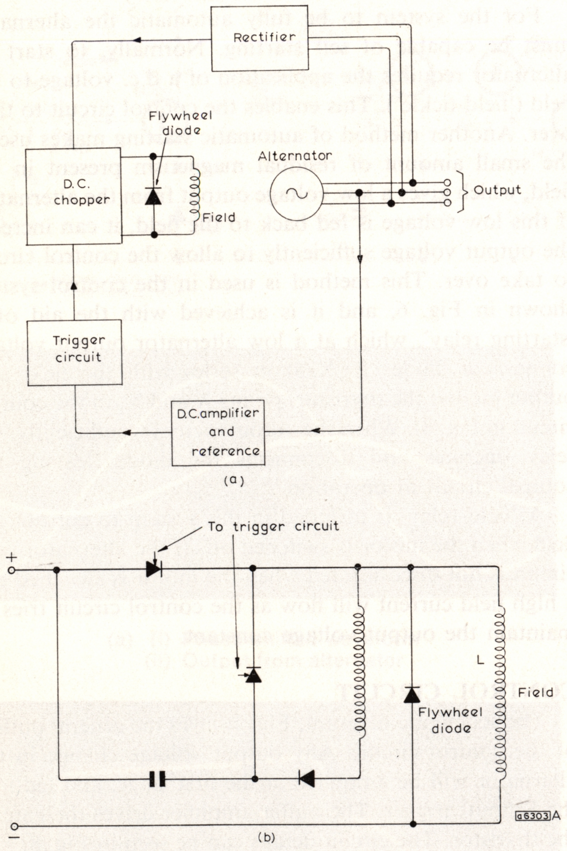

Rectifier
Flywheel diode
Alternator
Output
D.C. chopper
Field
Trigger circuit
D.C. amplifier and reference
(a)
To trigger circuit
+
L
Field
Flywheel diode
−
(b)

Fig. 4—(a) Voltage regulation control system: d.c. chopper
(b) D.C. chopper circuit using thyristors

Thyristor Phase Control

The thyristor phase control method (Fig. 5) combines fast response with reliable operation. It does not suffer from the disadvantages of frequent maintenance or of large sized components, and thus offers a considerable improvement over other methods in the performance of an alternator regulator set.

Thyristor phase control (Fig. 5) was chosen as the most suitable system, since it has distinct advantages over other methods. It uses a very compact control unit, which is capable of satisfying a major portion of all alternator applications. The mean output voltage can be adjusted easily by a potentiometer to suit the particular application.

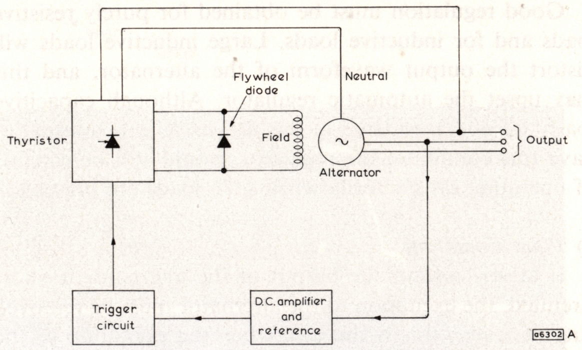

Flywheel diode
Neutral
Thyristor
Field
Alternator
Output
Trigger circuit
D.C. amplifier and reference

Fig. 5—Thyristor phase-controlled regulator

This permits any voltage between 70V and 400V to be set up, dependent upon the characteristics of the alternator. Good regulation can be maintained over the whole range by the use of a gain control potentiometer.

Better alternator output waveforms can be achieved with the d.c. chopper method, but the increase in performance is not considered to justify the extra expense for regulators controlling the majority of lower-powered alternators (below 30kVA).

CONTROL SYSTEM REQUIREMENTS

An alternator output voltage control system must be capable of doing three important things. Firstly, it must be able to decide that the output a.c. voltage has changed. Secondly, the change must be used to adjust the exciting field current to restore the output voltage to the desired level. It must be able to do this in the shortest possible time, without overshoot or oscillation. Thirdly, since an alternator will most probably be used in isolation away from mains and other apparatus, it must be capable of self-starting. The alternator must first produce an output voltage of adequate magnitude before the automatic system, which operates with this voltage as a power supply, is able to take command of the regulation.

In general, any system involving the rectification of the output voltage to obtain an error signal, or any system using devices similar to the saturable reactor, will be slow due to the inherently long time constants involved. Also, the system would be more bulky and more expensive than the system described in this article.

It is not intended to compare the different methods of automatic voltage regulators in detail, but to describe one which is cheap and reliable and meets the following performance requirements:

1) *Starting*

To be fully automatic the system must be capable of starting and controlling to a set output voltage, without having any external starting supply.

2) *Regulation with Loads*

The system must have a good voltage regulation when direct or line loads are applied. Voltage regulation of 3% can be considered adequate for general purpose alternators, with the possibility of obtaining regulation better than 1%.

3) *Load Condition*

Good regulation must be obtained for purely resistive loads and for inductive loads. Large inductive loads will distort the output waveform of the alternator, and this may upset the automatic regulator. Although capacitive loads are not considered in this article, as it is unusual to have this condition, the regulator should still be capable of operating satisfactorily when such loads are present.

4) *Fault Condition*

If at any instant the output of the alternator is short circuited, the excitation to the alternator must be removed automatically; this is the case when the excitation of the alternator is obtained directly from its output.

5) *Waveform Distortion*

Usually the field winding of an alternator, when used with an automatic voltage regulator, obtains its current directly from the alternator output. Under these conditions it is important that the output waveform should not be distorted to such an extent that it would be unacceptable for general use.

6) *Single-phase or Three-phase*

The regulator must be capable of operating on alternators which have single-phase or three-phase outputs.

PRACTICAL CONTROL SYSTEM

A schematic diagram of the overall control system to be described is shown in Fig. 6. On site an alternator will probably be driven by a diesel engine. For the experimental system a 5hp motor is used to drive a 4kVA, 400Hz alternator. Static contactors are used for switching the power supplies to the motor and for applying the load to the alternator, but mechanical contactors could be used instead.

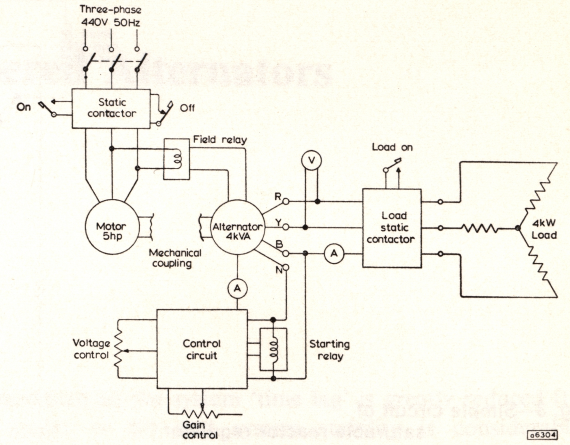

Three-phase
440V 50Hz
On
Static contactor
Off
Field relay
Load on
V
R
Y
B
N
Motor 5hp
Alternator 4kVA
Mechanical coupling
Load static contactor
4kW Load
A
A
Voltage control
Control circuit
Starting relay
Gain control
a6304

Fig. 6—Schematic diagram of alternator control system

For the system to be fully automatic the alternator must be capable of self starting. Normally, to start an alternator requires the application of a d.c. voltage to the field ('field tickle'). This enables the control circuit to take over. Another method of automatic starting makes use of the small amount of residual magnetism present in the field, which gives a low voltage output from the alternator. If this low voltage is fed back to the field, it can increase the output voltage sufficiently to allow the control circuit to take over. This method is used in the control system shown in Fig. 6, and it is achieved with the aid of a 'starting relay', which at a low alternator output voltage connects a diode (BYX25) in series with the field and output (across the thyristor, points X and Y, in the control circuit in Fig. 8). When the output increases sufficiently, the relay operates and disconnects the diode, leaving the control circuit in operation.

A 'field relay' is included in this system to cut out the field when the motor is switched off. If the alternator field circuit is not disconnected when the motor is switched off, a high field current will flow as the control circuit tries to maintain the output voltage constant.

CONTROL CIRCUIT

The schematic diagram, Fig. 7, gives the general outline of the control circuit. Any output voltage change in the alternator will be amplified at the first stage, and fed into the Schmitt trigger. The buffer amplifier drives the gate of the thyristor. The circuit details can be seen in Fig. 8.

The conduction angle of the thyristor controls the current passing through the field and is determined by the addition of two waveforms, the inverted half sinewave from the first transistor and the displaced waveform from the phase-shifting network (Fig. 9a). The inverted half sinewave from the collector of TR_1 is used in preference to a d.c. level, since a d.c. level would require a transformer, rectifiers, and a smoothing capacitor. In addition, to obtain the necessary alternator regulation transistor TR_1 would need to have a high gain to amplify any change in alternator output. To limit the amplified ripple on the d.c. level would require a large smoothing capacitor. This would reduce the response time of the system, and any ripple present would cause erratic triggering of the thyristor. The phase-shifting network was used at an angle of 60° so that the resultant waveform (Fig. 9b) closely approximated to a linear slope. This slope will vary directly with any change in output of the alternator.

Initially, TR_2 in the Schmitt trigger is conducting and the thyristor is non-conducting. When the input voltage increases positively (Fig. 9b) TR_2 cuts off at the Schmitt trigger level and turns on TR_3. The buffer amplifier TR_4 then conducts into the gate of the thyristor (Fig. 9c).

Only one rectifier, without smoothing, is required to supply the control circuit since the gate pulse is required only when the output of the alternator is positive. This enables the circuit to be used on single-phase or three-phase alternators.

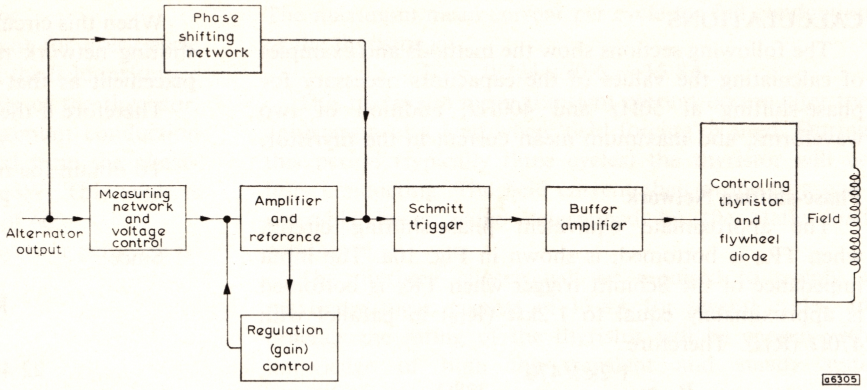

Phase shifting network
Alternator output
Measuring network and voltage control
Amplifier and reference
Schmitt trigger
Buffer amplifier
Controlling thyristor and flywheel diode
Field
Regulation (gain) control
a6305

Fig. 7—Schematic diagram of control circuit

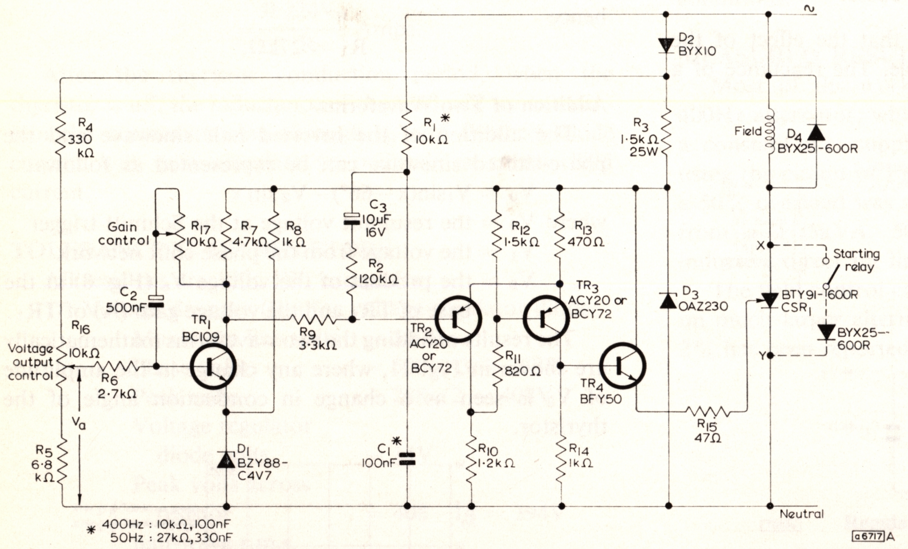
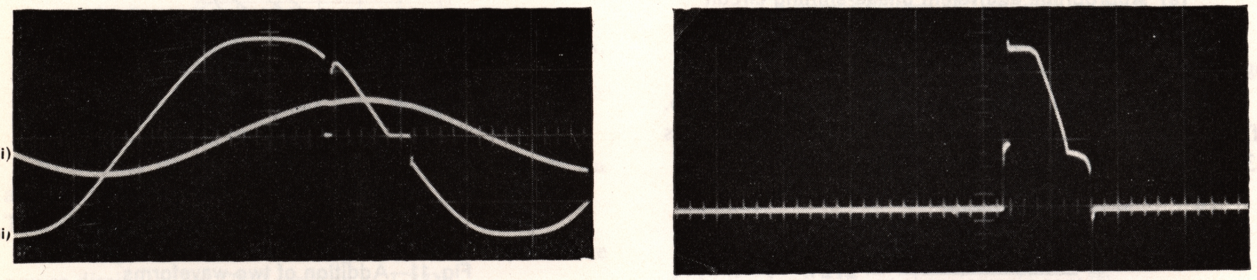
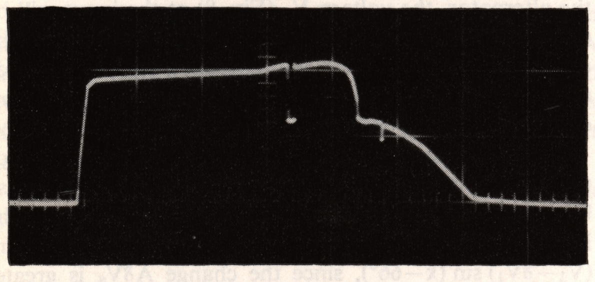

~
D2 BYX10
R4 330 kΩ
R1* 10kΩ
R3 1·5kΩ 25W
Field
D4 BYX25-600R
Gain control
R17 10kΩ
R7 4·7kΩ
R8 1kΩ
C3 10μF 16V
R2 120kΩ
R12 1·5kΩ
R13 470Ω
X
Starting relay
C2 500nF
TR1 BC109
R9 3·3kΩ
TR2 ACY20 or BCY72
TR3 ACY20 or BCY72
D3 OAZ230
BTY91-600R CSR1
BYX25-600R
R16 10kΩ
Voltage output control
R6 2·7kΩ
R11 820Ω
TR4 BFY50
Y
Va
R15 47Ω
R5 6·8 kΩ
D1 BZY88-C4V7
C1* 100nF
R10 1·2kΩ
R14 1kΩ
Neutral
* 400Hz : 10kΩ,100nF
50Hz : 27kΩ,330nF
a6717A

Fig. 8—Control circuit



(a) (i) Phase-shifted waveform
(ii) Output from alternator

(c) Gate pulse



(b) Addition of inverted and phase-shifted sinewaves

Fig. 9—Control circuit waveforms:

CALCULATIONS

The following sections show the methods and examples of calculating the values of the capacitors necessary for phase-shifting at 50Hz and 400Hz, addition of two waveforms, and maximum mean current in the thyristor.

Phase-shifting Network

The approximate equivalent phase-shifting circuit, when TR_2 is bottomed, is shown in Fig. 10a. The input impedance of the Schmitt trigger when TR_2 is bottomed is approximately equal to 1·2kΩ (R_{10}) in parallel with 470Ω (R_{13}). Therefore

$$R_s \simeq \frac{1{\cdot}2k \times 470}{1{\cdot}2k+470} = 338\Omega.$$

The capacitor C_1 is chosen so that the effect of the parallel loading R_2+R_s is negligible. The reactance of a 100nF capacitor at 400Hz = 4kΩ.

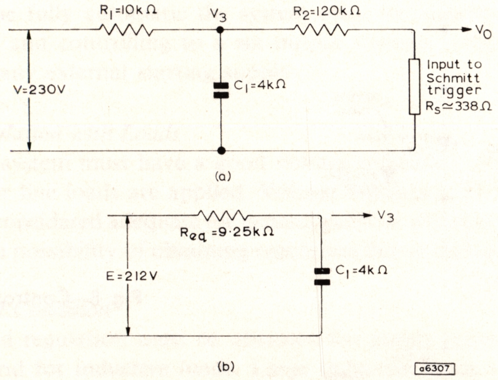


Fig. 10—Equivalent circuits of phase-shifting networks
(a) Appropriate equivalent phase-shifting circuit (TR_2 bottomed)
(b) Equivalent Thévenin's circuit

The equivalent Thévenin's circuit is shown in Fig. 10b. If, for example, the output voltage V of the alternator is 230V, the equivalent Thevénin's voltage E would be:

$$E = \frac{V \times (R_2+R_s)}{R_1+R_2+R_s}$$

$$= \frac{230 \times (120k+338)}{10k+120k+338} = 212V$$

where k indicates kΩ.

Equivalent resistance R_{eq} would be:

$$R_{eq} = \frac{R_1 \times (R_2+R_s)}{R_1+R_2+R_s}$$

$$= \frac{10k \times (120k+338)}{10k+120k+338}$$

$$= 9{\cdot}25k\Omega.$$

Hence V_3 across capacitor C_1 is:

$$V_3 = \frac{E(-jx_c)}{R_{eq}-jx_c} = \frac{212(-j4k)}{9{\cdot}25k-j4k}$$

$$= 33{\cdot}4-j77{\cdot}4$$

$$= 84{\cdot}5V \text{ (}V_3\text{ lagging 66° from V).}$$

Voltage at Schmitt circuit is:

$$V_0 = \frac{V_3 \times R_s}{R_2+R_s} = \frac{84{\cdot}5 \times 338}{120k+338}$$

$$= 0{\cdot}28V \text{ lagging } 66°.$$

When this circuit is required for use at 50Hz the phase-shifting network must be changed to give the same displacement as that obtained for 400Hz.

Therefore if the capacitor C_1 is 330nF:

$$x_c \text{ at } 50Hz = 9{\cdot}65k\Omega.$$

To obtain the required phase shift:

$$R_{eq} = 9{\cdot}65k\Omega \times \tan 66°$$

$$= 22{\cdot}4k\Omega.$$

Since

$$R_{eq} = \frac{R_1 \times (R_2+R_s)}{R_1+R_2+R_s}$$

$$22{\cdot}4k\Omega = \frac{R_1 \times (120k+338)}{R_1+120k+338}$$

hence

$$R_1 = 27k\Omega.$$

Addition of Two Waveforms

The addition of the inverted half sinewave and the phase-shifted sinewave can be represented as follows:

$$V_0 = V_1 \sin(x-66°) - V_2 \sin x$$

where V_0 = the resultant voltage at the Schmitt trigger
V_1 = the voltage from the phase-shift network
V_2 = the product of the voltage V_a (Fig. 8) at the base of TR_1 and the voltage gain (A) of TR_1.

The results of adding the two waveforms mathematically are shown in Fig. 11, where any change in the amplitude of V_2 is seen as a change in conduction angle of the thyristor.

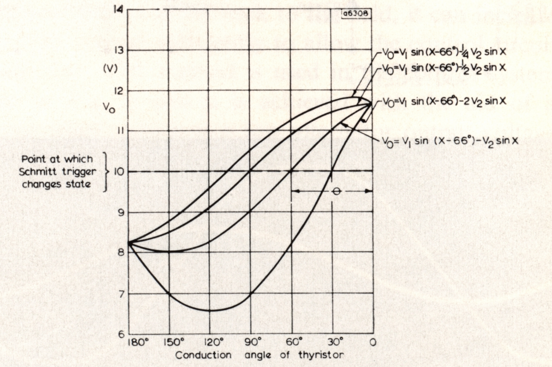


Fig. 11—Addition of two waveforms

When it is required to increase the output voltage of the alternator, the voltage V_a (Fig. 8) at the input will be decreased by a small amount δV_a, and hence V_2 will be decreased by $A\delta V_a$. This will cause V_0 to tend towards the waveform $V_1 \sin(x-66°)$, which increases the conduction angle and correspondingly the alternator current.

When a load is applied to the output of the alternator the voltages V_1 and V_a will decrease, and V_2 will decrease by an amount $A\delta V_a$. This will cause the voltage V_0 at the input of the Schmitt trigger to tend towards the waveform $(V_1-\delta V_1)\sin(x-66°)$, since the change $A\delta V_a$ is greater than the change δV_1. Hence the conduction angle increases and the output of the alternator will tend towards the set value.

The voltage regulation of the alternator is determined by the stage gain (A) of TR_1 and can be adjusted for positive or negative regulation by the gain control.

Maximum Conduction Angle of Thyristor

The maximum mean thyristor current for every cycle will depend upon the peak voltage (V_p), the field resistance (R) and the maximum conduction angle of the thyristor. In this particular application the maximum conduction angle cannot exceed the angle obtained from the phase-shifting network (Fig. 11), when V_2 = 0V. This angle is approximately 114°, or a trigger angle of 66°.

Hence the mean current I_m in the thyristor per cycle is:

$$I_m = \frac{V_p}{R}\int_0^{114°} \frac{\sin x}{2\pi}\,dx$$

$$= \frac{V_p}{2\pi R}(1{\cdot}406)$$

$$= \frac{0{\cdot}224V_p}{R} \text{ Amps.}$$

After the thyristor conduction period, when the thyristor is off, the inductance of the field will try to maintain the current passing through it, and flywheel diode current will then circulate to maintain a steady field current.

TOLERANCING OF RESISTORS

All resistors are 10% ¼W, except for:

1) Voltage dropper (R_3) for voltage regulator diode:

Maximum line volts = 500V
Phase volts = 500/√3 = 288V
Peak volts = 288√2 = 408V
Voltage regulator diode volts = 14V
Peak volts across resistor = 408−14 = 394V
half-wave r.m.s. voltage = 197V
Current in 1·5kΩ dropper resistor = 197/1·5kΩ = 131mA.
Therefore maximum power dissipated = 25·8W

2) Phase-shifting resistor (R_1):

At 400Hz, from *Calculations* (page 38) the voltage V_R across the 10kΩ resistor = tan 66° × 84·5V = 195V. Therefore power dissipated = 3·8W.

Similarly, at 50Hz the voltage V_R = 195V, and the power dissipated in 27kΩ resistor = 1·33W.

CHOICE OF THYRISTOR

The choice of thyristor will depend upon the field requirements of the alternator. For example, the 3·75kVA alternator used had an exciter voltage of 24V and field resistance of 5Ω at 4·8A. The residual voltage output was approximately 1V r.m.s. This is a low output; most alternators will give a higher output, about 5V.

If the maximum output voltage is 250V, then the peak voltage will be 353V.

Hence the peak current = 353/5 = 70·6A.

The maximum mean current per cycle for full conduction of the thyristor is:

$$I_m = 0{\cdot}224 \times 70{\cdot}6 = 15{\cdot}8A.$$

This maximum mean transient current occurs after the application of a load when 'field forcing' is used. During this period (typically three cycles) the thyristor will be fully conducting. The field current then drops to a considerably lower value determined by the static load conditions.

The thyristor chosen will be required to supply a maximum mean current of 15·8A for several cycles. In practice the rating of the thyristor will be chosen with knowledge of both the transient and steady state conditions.

MEASURED RESULTS

Most of the work was carried out on a 3·75kVA, 400Hz alternator, which gave a regulation of 12·5% with a constant d.c. supply to the field. With field control, using the circuit of Fig. 8, a regulation better than 1% at a 50% overload was achieved. Measured results obtained from a 1·75kVA, 50Hz alternator with resistive and inductive direct on line loads are shown in Table 1.

The field control circuit has also been used successfully on much larger alternators (30kVA), and a regulation of 2% has been reported.

TABLE 1

Regulation of Output Voltage

Results on an H. J. Scott, 50Hz 1·75kVA alternator at a set output voltage of 210V with no load.

Load		Output voltage on load	Change in output voltage with load
Resistive (W)	Inductive (motors) (hp)	(V)	(%)
Resistive load.			
0	—	210	—
700	—	210	0
1400	—	210	0
2000	—	208	−0·9
Inductive load, without changing gain control.			
—	0·25	213	+1·4
—	0·5	214	+1·9
—	0·25+0·5	213	+1·4
Complex load, without changing gain control.			
700	0·25	211	+0·5
1400	0·25	210	0
2000	0·25	220	+4·8
700	0·25+0·5	211	+0·5
1400	0·25+0·5	210	0

The regulation with inductive or complex loads can be improved to better than 1% by adjustment of the gain control.

Voltage Transient and dV/dt Suppression in Thyristor Bridges

J. Merrett

Mullard Central Application Laboratory

Voltage transients on the supply mains and rapid rates of rise of voltage during switching can cause thyristors to turn on. Such uncontrolled triggering can lead to device failure or undesirable rotation of a motor for example. Suppression circuits can be used at the input to a thyristor bridge and also across individual thyristors in order to reduce or eliminate these undesirable effects. The design of these circuits and a number of practical results are discussed in this article.

INTRODUCTION

Power semiconductor devices are basically robust devices and are capable of handling considerable transient current overloads. The avalanche types can also withstand high energy transients in the reverse direction.

Thyristors, however, will be switched to their forward conducting state if the forward voltage across them exceeds the forward breakover voltage (V_{BO}) or if a voltage less than this is applied with a rate of rise greater than the rated maximum value (dV/dt max). The thyristor may not be damaged by being turned on in this way provided that the load current which follows does not exceed the rated maximum for the device.

In some applications, particularly those concerned with the speed control of d.c. shunt motors, the current following random thyristor triggering of this type can be very large, resulting in destruction of thyristors or rectifiers, or even damage to the motor. In such cases it is imperative that circuit measures should be taken to prevent such transient voltages reaching the thyristors.

Before circuits can be devised to suppress these transients it is necessary to know something of their nature and source impedance. The results of measurements made on supply mains and on the performance of a number of suppression circuits for both single and three phase mains are described in this article. The theoretical basis for the design of these circuits is also considered.

NATURE OF THE PROBLEM

Before considering circuit details it will be helpful to examine a number of basic practical bridge circuits and their supply and load connections. Four methods of connection are used for single phase inputs as shown in Figs. 1, 2, 3, and 4.

The line to neutral connection of Fig. 1 is the most common and is used for most low power systems. The circuit of Fig. 2 is used either when a higher power is required or where a fully rated neutral is not available. An auto transformer as shown in Fig. 3 is sometimes used for lower power systems up to 2 or 3kW where a line to neutral system would normally have been used but where a neutral is not always available. The double wound transformer of Fig. 4 may be used with line to line or line to neutral systems when isolation from the supply is important.

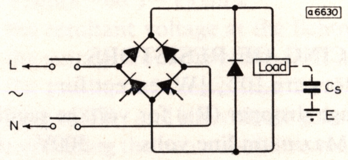


Fig. 1—Bridge with single phase input, connected line to neutral

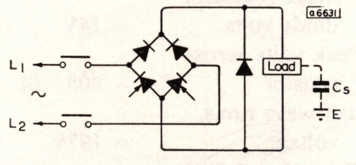


Fig. 2—Bridge with single phase input, connected line to line

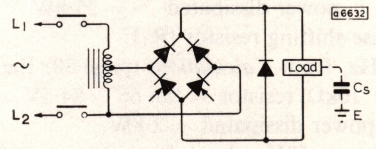


Fig. 3—Bridge with single phase input, connected line to line via auto transformer

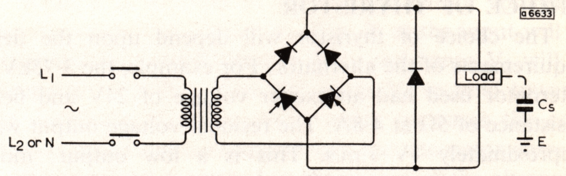


Fig. 4—Bridge with single phase input, connected line to line or line to neutral via double wound transformer

Many different d.c. loads are possible, but the most common, with which we shall be primarily concerned, is the d.c. shunt wound motor. The armature is usually supplied direct from the thyristor bridge, and the field separately excited from a separate small uncontrolled diode bridge.

Motor armatures usually have a relatively low resistance and a time constant between about 10 and 20ms. The armature resistance of motors from about 1 to 50 hp will be such as to permit a stalled motor current of at least 20 times the normal full load rated current. When we are considering the bridge circuit, particularly when all thyristors are in the non-conducting state, the load, to a first approximation at least, may be considered to be a short circuit with a distributed stray capacitance C_s to earth.

The thyristor stack will usually be connected to the supply through a mains contactor. This will always be of the double pole type when the line to line connection is used, but may sometimes be of the single pole type with a solid neutral when the stack is connected between line and neutral.

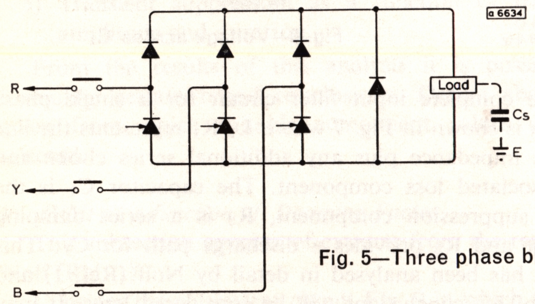


Fig. 5—Three phase bridge

Three phase bridges are mostly used at higher powers, and power transformers are rarely incorporated in motor drive systems. We will therefore consider only the circuit shown in Fig. 5, although the factors governing the design of single phase systems with transformer can equally well be applied to three phase systems.

Random Line Transients

The mains voltage will consist of the 50Hz sinewave with superimposed random transients.

If the peak voltage of a transient, when added to the instantaneous supply voltage, exceeds the thyristor V_{BO}, the thyristor will turn on. It is therefore necessary to devise some suppression circuit to limit the peak transient voltage to a safe level. At the same time a thyristor should be chosen with a V_{BO} considerably higher than the crest repetitive supply voltage so that there is an adequate voltage margin to allow for supply voltage changes and for the residual transients after suppression.

Unfortunately, the precise nature of these random transients is not yet known, although statistical evidence is continually being collected as to the voltage amplitude, energy level, and frequency of occurrence of these transients in a number of locations all over the country. It has already been fairly conclusively established that these transients follow a certain pattern in so far that the high voltage spikes are of much shorter duration than the lower voltage transients and on the whole are of lower energy level.

Local Switching Transients

Local switching transients are generated by the operation of the mains contactor on the equipment itself and cause trouble in two ways. The contactor will close very rapidly and at a completely random time in relation to the supply waveform. If the contacts close at the crest of the supply voltage this voltage will be applied to the bridge with a very rapid rate of rise, often as high as 1000V/μs. This rate of rise is sufficient to turn on all but the fastest of thyristors. Alternatively, if the supply is inductive, either because a line choke is used or because of the leakage inductance of a transformer, and some transient suppression capacitance is used across the thyristor bridge input, the series L-C combination can ring to produce a considerable voltage overswing.

The suppression of both the random and local switching transients can take the same circuit form, so that it is desirable to consider both requirements when designing such circuits.

POWER SOURCE IMPEDANCE

The Electrical Research Association have been engaged in work associated with radio interference and mains borne transients, for which they have designed a portable equipment for measuring mains source impedance over a broad frequency band. We were able to borrow this equipment for a short time during which the mains impedance in several widely differing situations was measured. These results have been compared with similar measurements made by ERA in other parts of the country and were found to agree quite closely. It is therefore concluded that our results may be treated as representative.

The measurements were made under the following conditions.

1) At the socket outlet of a domestic 30A ring main.
2) At the outlet of a 60A supply in an industrial research laboratory about 100 metres from a substation transformer.
3) At the terminals of an unloaded 750kVA substation transformer which was itself fed directly from an 8MVA transformer from the 132kV grid. The two transformers were not more than 10 metres apart.

The results of these measurements are shown graphically in Fig. 6, where impedance is indicated in dB relative to 1Ω. For convenience the impedance values in ohms are also shown against each main scale division.

It will be seen in each case that initially the characteristic is linear with a slope of about 6dB per octave, or a little less, indicating a nearly pure inductive source. At higher frequencies the curve exhibits the usual transmission line characteristics.

At a frequency of 10kHz the apparent source inductance is as follows:

1) domestic 50μH
2) laboratory 72μH
3) transformer 32μH.

Typical armoured power cable has a characteristic impedance of 75Ω and an inductance of about 10μH per 100 metres.

As a further check on these results it is interesting to note that if the 750kVA transformer had a 5% reactive voltage drop the series inductance would be 40μH. This compares well with the measured value of 32μH.

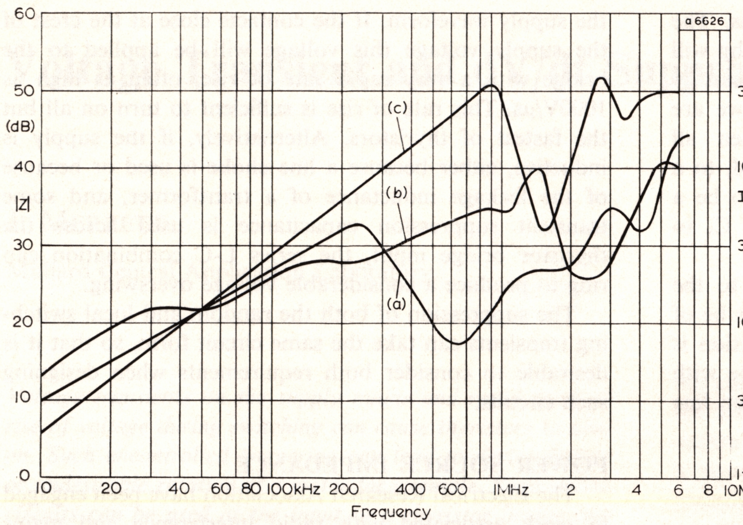


Fig. 6—Source impedances measured as dB relative to 1Ω
(a) Domestic 30A ring main (line to neutral 240V) Ashtead, Surrey, 8 April 1967
(b) Industrial laboratory 60A mains (line to neutral 230V) Loughborough, Leics, 7 April 1967
(c) Secondary of 750kVA transformer on no load (1000A, 268V line to neutral) Loughborough, Leics, 7 April 1967

The source impedance remote from the transformers is likely to be greater than this but will be modified by the shunt load connected to the supply. In the case of the domestic supply where the shunt load is likely to be mainly resistive and the substation was 300 metres away, the additional inductance would be primarily due to cable inductance. This would amount to about 30μH which with say 30μH for the transformer gives a total of 60μH, again comparing quite well with the measured value of 50μH.

From these results it may be assumed with some degree of confidence that the source impedance of normal supply mains will mostly consist of inductive reactance between frequencies of 10 and 100kHz. This inductance will be greater than about 40μH and probably not more than about 80μH. If power factor correction capacitors are used on the load side of the local substation transformer the above general conclusion will almost certainly not be true, and such cases should be treated individually.

The characteristics of the supply above about 100kHz are not generally of any interest as it is essential to filter out all high frequency components before they reach the thyristor bridge.

BRIDGE INPUT SUPPRESSION

Most of the random and local switching voltage transients can be removed, or reduced to a safe level, by a suitable shunt capacitor across the a.c. input terminals of the bridge. The detailed design of this type of input suppression filter will be considered in this section. It should, however, be remembered that individual device suppression is often necessary in addition to input circuit suppression for reasons which will be described in detail in the next section. As the design of the individual suppression circuits has very little effect upon the input circuit design, the two circuits can be considered separately.

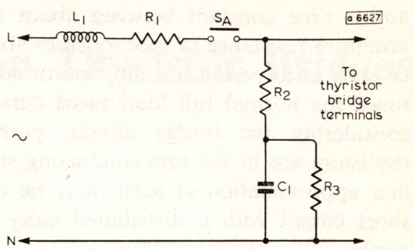


Fig. 7—Input filter for single phase system

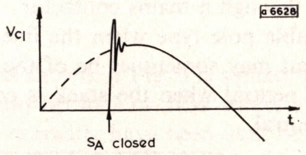


Fig. 8—Voltage across C_1

The complete input filter circuit for a single phase system is shown in Fig. 7 where L_1 R_1 represents the line source impedance plus any additional series choke and its associated loss component. The capacitor C_1 is the shunt suppression component, R_2 is a series damping resistor and R_3 provides a discharge path for C_1. This circuit has been analysed in detail by Nolf (Ref. 1) and some of his conclusions will be considered later. It may however be helpful to examine the operation of this circuit in more general terms in order to gain some understanding of its operation.

In most cases, as we have seen in the preceding section, the line impedance is largely inductive so that at frequencies above a few kHz we have:

$$\omega L_1/R_1 > 1.$$

When the thyristors in the bridge are in their non-conducting state and the mains contactor S_A is closed, a series resonant circuit is formed of L_1C_1 with series damping R_1+R_2. If the loss components of this circuit are small the circuit will ring and the voltage appearing across C_1 will exceed the supply voltage as shown in Fig. 8. If R_2 is zero or very small, most of this ring voltage will appear across the bridge input and may result in the forward breakover of a thyristor, although the presence of C_1 may have effectively slowed down the rate of rise of voltage to a safe value of dV/dt. It is therefore most important to ensure that the combined value of R_1 and R_2 is large enough to provide sufficient circuit damping.

Unfortunately, too large a value of R_2 reduces the effectiveness of C_1, and it is not easy to make R_1 large. It is clearly not possible to make R_1 a physical resistance as the power losses would be too large, but it is sometimes possible to make this the series loss component of a choke which has negligible loss at 50Hz but a useful loss at higher frequencies. Because of these difficulties a compromise has to be made between acceptable damping and filtering efficiency, a subject which forms a large part of Nolf's report.

In many cases the supply impedance will be known only to lie between broad limits so that no accurate design will be possible. Alternatively a series choke may be used to swamp the supply inductance and provide a better defined input circuit. The final choice will probably be dictated by economic considerations, and in low power systems the choke is quite often omitted.

Circuit Design Theory

The input suppression circuit has to be designed to limit dV/dt on switch-on, and to have an acceptable voltage overshoot and a known ability to absorb random supply voltage transients.

The circuit analysis will be described under the following subsections:

1) dV/dt as a function of damping factor
2) Voltage overshoot as a function of damping factor
3) Filter output voltage as a function of choke loss factor
4) dV/dt as a function of choke loss factor
5) Transient suppression as a function of transient amplitude and duration.

From the results of this analysis it is possible to formulate certain broad conclusions. Design abacs are given from which suitable component values can be selected.

1) *dV/dt as a function of Damping Factor*

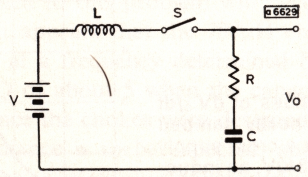
This subsection consists of extracts from the report by Nolf (Ref. 1).

Consider the equivalent circuit Fig. 9 in which the a.c. supply has been replaced by a battery of voltage V, where in practice:

V = crest supply voltage.

We are concerned with the output voltage V_o immediately after the closing of switch S.

Fig. 9—Equivalent suppression circuit



It can be shown that:

$$\frac{dV_o}{dt} = \left\{\frac{\omega_n V}{\sqrt{(1-\eta^2)}}\exp(-\eta\omega_n)t\ \sin(\omega_n\sqrt{(1-\eta^2t)}+2\phi)\right\} \qquad \ldots(1)$$

where $\omega_n = 1/\sqrt{(LC)}$; damping factor $\eta = R/(2\omega_n L)$; $\phi = \text{arc sin}\ \eta$.

The time t_c at which this expression has a maximum value is given by:

$$t_c = (\tfrac{1}{2}\pi - 3\ \text{arc sin}\eta)/\omega_n\sqrt{(1-\eta^2)} \qquad \ldots(2)$$

It can be shown that t_c takes negative values for $\eta \geqslant 0{\cdot}5$, so we only need consider the interval $0 \leqslant \eta \leqslant 0{\cdot}5$.

The solutions of Eq. 2 for times t_c between 0 and $\pi/2\omega_n$ are shown graphically in Fig. 10.

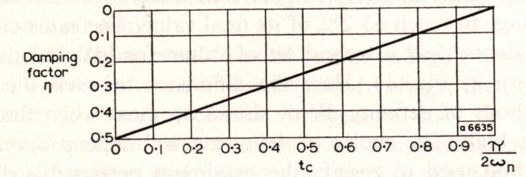


Fig. 10—Solutions of Eq. 2 for $0 \leqslant \eta \leqslant 0{\cdot}5$

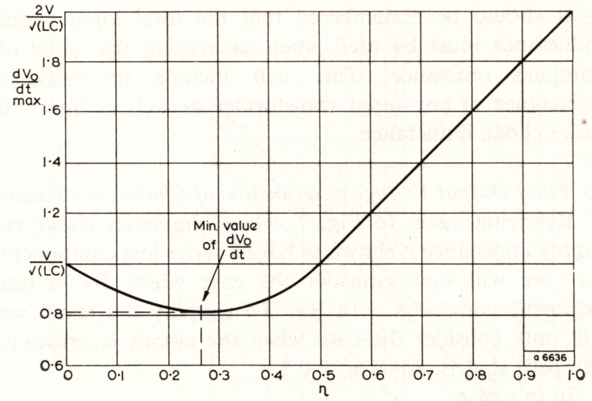


Fig. 11—Solutions of Eq. 3 for $\eta = 0$ to $\eta = 1{\cdot}0$

To find the maximum value of dV_o/dt, substitute the value of $t = t_c$ from Eq. 2 into Eq. 1, which gives:

$$(dV_o/dt)_{max} = \omega_n V\exp[\eta/\sqrt{(1-\eta^2)}](\tfrac{1}{2}\pi - 3\ \text{arc sin}\eta) \qquad \ldots(3)$$

for $0 \leqslant \eta \leqslant 0{\cdot}5$.

For the special case $\eta = 0{\cdot}5$

$$(dV_o/dt)_{max} = 2\eta\omega_n V \qquad \ldots(4)$$

$$= (R/L)V \qquad \ldots(5)$$

or

$$(dV_o/dt)_{max} = V[1/\sqrt{(LC)}]. \qquad \ldots(6)$$

The solutions of Eq. 3 for a range of values of η are shown graphically in Fig. 11, from which it may be seen that the minimum value of $(dV_o/dt)_{max}$ occurs when $\eta \simeq 0{\cdot}265$. Under these conditions:

$$(dV_o/dt)_{max} = 0{\cdot}81V(R/L) \qquad \ldots(7)$$

$$= 0{\cdot}81V[1/\sqrt{(LC)}] \qquad \ldots(8)$$

2) *Voltage Overshoot as a function of Damping Factor*

This subsection consists of extracts from the report by Nolf (Ref. 1).

It can be shown that the instantaneous output voltage from the equivalent circuit of Fig. 9 is given by:

$$V_o = V\{1-[\exp(-\eta\omega_n t)/\sqrt{(1-\eta^2)}]\cos[\omega_n\sqrt{(1-\eta^2)}t+\phi]\}. \qquad \ldots(9)$$

The value of V_o has a maximum value when:

$$t = (\pi-\phi)/\omega_n\sqrt{(1-\eta^2)}. \qquad \ldots(10)$$

Substitution of Eq. 10 in Eq. 9 gives:

$$V_{o(max)} = V\{1+[1/\sqrt{(1-\eta^2)}]\exp[-\eta/(1-\eta^2)][\pi-\text{arc sin}\eta]\} \qquad \ldots(11)$$

This peak voltage V_p may be expressed as a percentage overshoot of the applied voltage V:

$$V_p = [100/\sqrt{(1-\eta^2)}]\exp[-\eta/\sqrt{(1-\eta^2)}][\pi-\text{arc sin}\eta]\% \qquad \ldots(12)$$

The values of V_p for a range of values of η are shown graphically in Fig. 12.

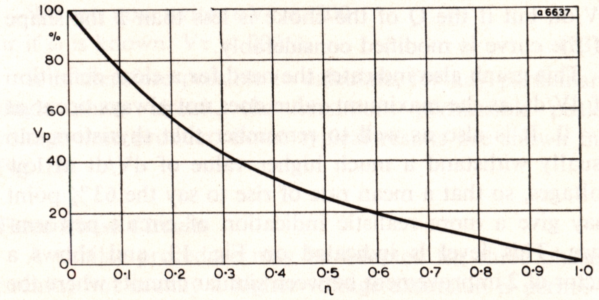


Fig. 12—Percentage overshoot V_p for $\eta = 0$ to $\eta = 1{\cdot}0$

It should be remembered that the total input series inductance must be used when calculating the value of damping resistance. This will include the leakage inductance of any input transformer as well as line and series choke inductance.

3) *Filter Output Voltage as a function of Choke Loss Factor*

Referring again to Fig. 7, where the series choke or supply impedance is shown to have a series loss component R_1, we will now consider the case where R_1 is not negligible compared with R_2. To simplify the result we will only consider the case when the circuit is critically damped; that is, when $\eta = 0{\cdot}5$.

In this case

$$\eta = (R_1+R_2)/2\omega L_1 \qquad \ldots(13)$$

It can be shown by normal circuit analysis methods that the instantaneous output voltage is given by:

$$V_o = V[1-\exp(-\omega t)][(\omega t/Q)+1] \qquad \ldots(14)$$

where

$$\omega = \frac{1}{\sqrt{(L_1C_1)}} \qquad \ldots(15)$$

and

$$Q = (\omega L_1)/R_1\,; \qquad \ldots(16)$$

that is, Q is the quality factor of the series choke.

Equation 14 has been evaluated for a range of values of Q from Q = 1 to Q = 8. The results are shown graphically in Fig. 13.

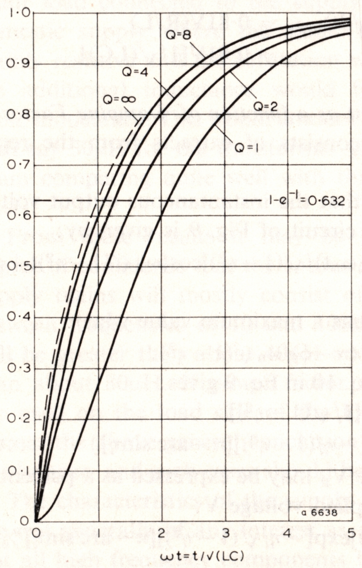


Fig. 13—Solutions of Eq. 14 for Q = 1, 2, 4, and 8

It will be seen that for chokes with a Q of more than 8 there is very little change in voltage rise or maximum dV/dt, but if the Q of the choke is less than 2 the shape of the curve is modified considerably.

This graph also indicates the need for a clear definition of dV/dt, as the maximum value does not always occur at t = 0. It is also as well to remember that thyristors can usually withstand a much higher value of dV/dt at low voltages, so that a mean rate of rise to say the 63% point may give a more realistic indication of circuit performance. This level is indicated on Fig. 13, and shows a factor of 2 improvement between similar circuits where the Q of the choke is either high or unity. It may therefore be possible to introduce useful circuit economies by intentionally introducing high frequency loss into the series choke and thereby reducing the size of the shunt capacitor or inductance of the choke that is required to achieve a given value of mean dV/dt.

4) *dV/dt as a function of Choke Loss Factor*

By differentiating Eq. 14 we obtain:

$$dV_o/dt = \omega V\{\exp(-\omega t)[(1/Q)(\omega t-1)+1]\} \ldots(17)$$

For values of $Q \geqslant 2$ the maximum real value of this expression occurs at time $\omega t = 0$. When $Q = 1$ the maximum dV_o/dt is at $\omega t = 1$.

In the general case for $Q \geqslant 2$:

$$(dV_o/dt)_{max} = \omega V[1-(1/Q)] \qquad \ldots(18)$$

and for the particular case $Q = 1$,

$$(dV_o/dt)_{max} = 0{\cdot}368\omega V.$$

Values of $(dV_o/dt)_{max}$ for a crest supply voltage of 340V, an inductance of 500μH, and a capacitor of 4μF, all with the circuit critically damped, are shown graphically in Fig. 14. There are no values for $Q < 1$ as in such cases the circuit would become overdamped and the boundary condition would not be valid. This graph clearly shows the advantage to be gained from the use of a choke with high losses, and also that for $Q > 5$, say, the losses may to a first approximation be neglected and the analysis due to Nolf will be valid, at least for circuits with component values of this order of magnitude.

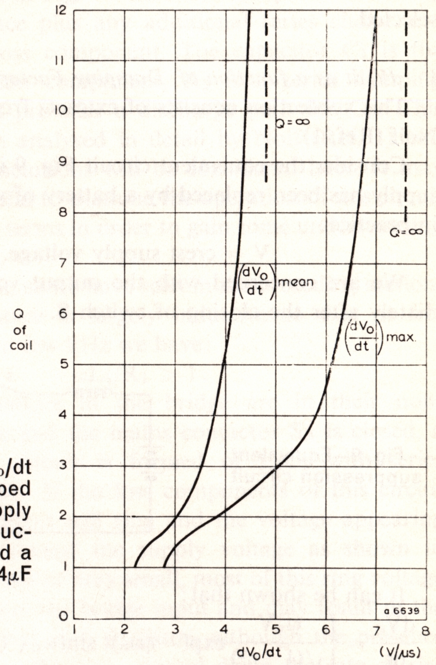


Fig. 14—Values of dV_o/dt for a critically damped circuit with a crest supply voltage of 340V, an inductance of 500μH, and a capacitor of 4μF

So far we have been concerned with the maximum value of dV/dt. Alternatively, we may specify the rate of rise of voltage in terms of the apparent time constant of the circuit; that is from the time taken for the output voltage to reach 63·2% of its final value. The same circuit constants yield a second set of values for $(dV_o/dt)_{mean}$ as shown in Fig. 14. Here the difference between the two methods of defining dV/dt shows up most when the coil Q is high. The choice of definition will depend upon the method used to specify the maximum permissible dV/dt value for the thyristor.

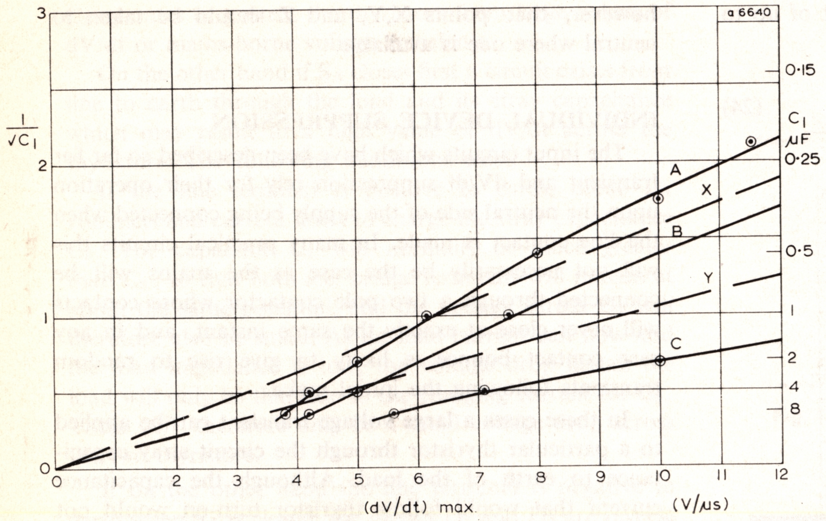


Fig. 15—Measured values of $(dV/dt)_{max}$ for iron cored chokes rated at full line current, with theoretical values (broken lines) for comparison

	L_1	R_2	Rating	Q
A*	780μH	22Ω	36A	
B*	520μH	22Ω	70A	
C*	60μH	3Ω	200A	
X	780μH	22Ω		2
Y	780μH	22Ω		5

*approximately critically damped

Some measured results are shown in Fig. 15, all for iron cored chokes rated at the full line current. Curve A may be compared with theoretical curves X and Y. From an examination of these curves the difficulties associated with a theoretical approach to this problem will become apparent. For example it appears that the 780μH choke (A) has a Q of about 2 at a frequency determined by a 1·0μF capacitor, and a Q of about 5 when the capacitor is increased to 6·0μF. Since the chokes were designed for use at 50Hz this performance is to be expected, and in fact can be put to good use as relatively smaller capacitors can be used for a given dV/dt. On the other hand, unless a considerable amount of information is available about choke loss at high frequency it is difficult to predict the performance of a particular circuit with any accuracy.

It is possible, and in some cases desirable, to use air cored chokes, the performance of which can be obtained more accurately; but the high frequency losses will be lower, requiring a larger capacitor, thus both the capacitor and choke will almost certainly be more expensive.

5) *Transient Suppression as a function of Transient Amplitude and Duration*

The bridge input inductance capacitance filter serves two purposes. It reduces dV/dt on switch-on and reduces the amplitude of random voltage transients which may occur on the mains.

If the maximum rate of rise of output voltage from the filter is known in terms of crest applied voltage, then the time taken to reach a certain voltage level may be calculated. The relationship between peak transient voltage, transient duration, and output voltage may therefore be established.

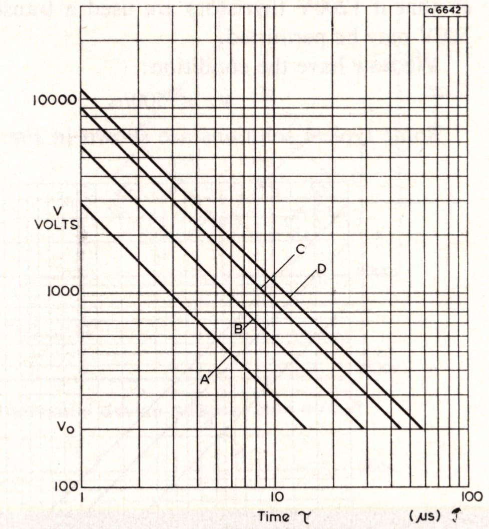


Fig. 16—Maximum permissible transient peak voltage-time product for single phase 240V circuits using 600V thyristors

	L_1	C_1	Q
A	50μH	4μF	∞
B	200μH	4μF	∞
C	500μH	4μF	∞
D	500μH	4μF	5

For a given critically damped filter circuit:

$$(dV_o/dt)_{max} = \omega V[1-(1/Q)] \qquad \ldots(19)$$

where

$\omega = 1/\sqrt{(L_1C_1)}$
Q = Q factor of series choke
V = crest supply voltage.

For most input circuits $Q \gg 1$, therefore

$$(dV_o/dt)_{max} \simeq \omega V. \qquad \ldots(20)$$

Now consider an applied transient of amplitude V and duration τ. The maximum output voltage is given by:

$$dV_o/dt = \omega V \qquad \ldots(21)$$

$$V_o = \omega V\tau. \qquad \ldots(22)$$

In practice it will be necessary to keep the value of V_o below a certain maximum value such that the crest supply voltage plus V_o is always less than the forward breakover voltage of the thyristors.

For a 240V single phase supply it is normally satisfactory to use 600V thyristors. Allowing for a 6% rise in supply voltage, the crest supply voltage becomes 360V, so that the maximum possible transient is 240V. To allow a certain margin of safety, take the maximum permissible transient voltage input to the bridge as 200V; that is, $V_{o(max)} \leqslant 200V$.

We can now write: $\omega V\tau \leqslant 200$

or if ω is known: $V\tau \leqslant 200/\omega$. $\qquad \ldots(23)$

It is therefore possible to calculate, for any particular single phase circuit, the maximum permissible peak voltage-time product. Some typical results are shown in Fig. 16.

Three Phase Circuits

A similar procedure may be adopted for three phase circuits, but usually a higher voltage excursion is permissible. The crest voltage of a 440V supply +6% is 660V, so that if 1200V thyristors are used a transient of up to 500V may be permitted.

We now have the condition:

$$V\tau \leqslant 500/\omega. \qquad \ldots(24)$$

Some typical solutions are shown in Fig. 17.

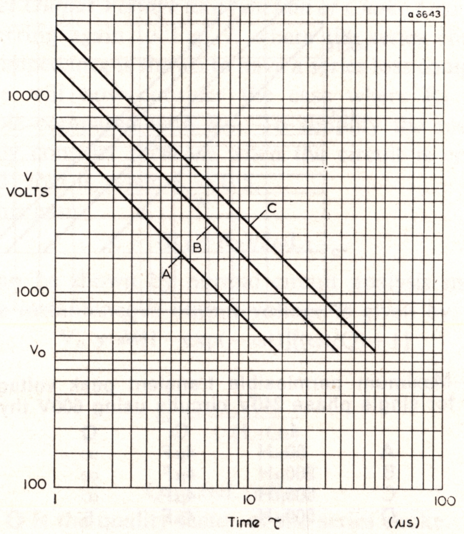


Fig. 17—Maximum permissible transient peak voltage-time product for three phase 440V circuits using 1200V thyristors

	L_1	C_1	Q
A	50μH	4μF	∞
B	200μH	4μF	∞
C	500μH	4μF	∞

All that has been said in the preceding parts of this section concerning single phase systems applies equally to three phase, particularly when the suppression network is connected between each line and a common neutral.

When a neutral is not available the input suppression circuits may be connected from line to line as shown in Fig. 18, and to some extent are equivalent to the single phase line to line circuit. A complete analysis of this system has not been carried out, but measured results correspond very closely with those obtained from the single phase line to line analysis. It is recommended, however, that points X,Y, and Z should be taken to neutral where one is available.

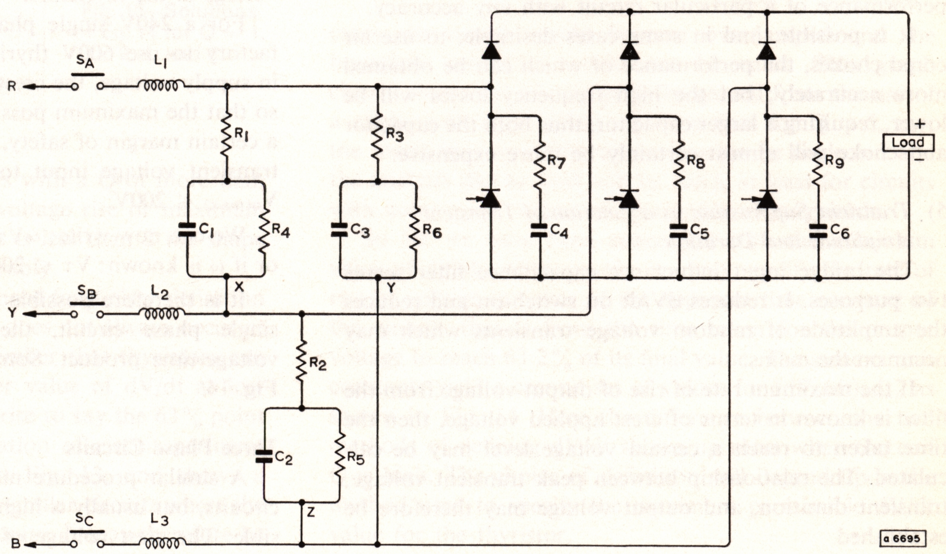


Fig. 18—Suppression circuit for use with three phase bridge.

INDIVIDUAL DEVICE SUPPRESSION

The input circuits which have been described so far for transient and dV/dt suppression rely for their operation upon the neutral side of the supply being connected when the line contact is made. In many practical circuits this will not necessarily be the case as the mains will be connected through a two pole contactor whose contacts will never close at exactly the same instant, and in any case contact bounce is likely to give rise to random transients following the initial make.

In these cases a large voltage transient can be applied to a particular thyristor through the circuit stray capacitance to earth of the load. Although the capacitance current that would follow thyristor turn-on would not sustain thyristor conduction, this initial charging current may be immediately followed by the closing of the neutral contact so that full conduction into the load can follow.

Spurious turn-on by this process requires a certain sequence of events in the contactor to occur near the crest supply voltage. Such a sequence of events may only arise, say, once every 100 operations; but if it can happen and the consequences of this are the destruction or premature ageing of thyristors, or perhaps some undesirable rotation of the motor, preventive measures must be taken.

It has been found that a series combination of capacitance and resistance connected across each thyristor effects a complete cure and reduces initial dV/dt in all known cases to a safe level. This arrangement alone will not be sufficient to attenuate input voltage transients, so that both suppression circuits will normally be required except where the neutral is not switched.

Circuit Conditions with Open Circuit Neutral

We will now consider the design of the individual device suppression circuit shown in Fig. 19.

If the contactor contact S_B closes before S_A and remains closed, then the input suppression circuit L_1, R_1, C_1 operates to protect the thyristors from large values of dV/dt or mains-borne voltage transients.

On the other hand if S_A closes first a circuit exists from line to earth through the load and its stray capacitance which may result in a high value of dV/dt across the thyristors. The following conditions exist.

If the line terminal is positive to earth, diode D_1 conducts and current flows to charge the stray capacitance C_s. The capacitor C_1 will normally be much greater than C_s, so that both a.c. bridge terminals will remain at about the same potential, and the voltage across D_2 will therefore also be small. As no load current can flow and the load impedance is low, the voltage drop across the load will only be that due to the charging current for C_s. There will therefore only be a small voltage drop across the two thyristors.

If on the other hand the line terminal is negative to earth when S_A is closed, the diodes D_1 and D_2 are reverse biased and nearly all the mains voltage appears across the two thyristors in the forward direction. The rate of change of forward applied voltage can be as high as 1000V/μs if the switch is closed when the mains supply is near to its crest voltage. By connecting capacitors C_2 and C_3 across the two thyristors the rate of rise of voltage across either thyristor can be reduced to an acceptable level. Some series resistance R_3 and R_4 must also be included to limit the peak capacitor discharge current when the thyristors are triggered into conduction. High peak currents could damage the thyristors by exceeding the rated value of dI/dt during the switch-on period. A practical upper limit of capacitance is about 0·5μF, and a 10Ω resistor will in most cases limit peak discharge current to a safe level. A lower limit is difficult to define on the basis of dV/dt protection alone, but a minimum value of 0·05μF is probably a good compromise.

dV/dt with Individual Device Suppression

Before proceeding further it will be as well to consider the effects of these components on the normal operation of the circuit with the neutral contact making first, or with a solid neutral connection.

Consider the case of the line being positive when S_A (Fig. 19) is closed. Diode D_1 will conduct, and as the load has a very low impedance compared with the forward leakage of the other components of the thyristor bridge, nearly all the mains voltage will appear across the thyristor CSR_2. Because of the low voltage drop across the load the voltage difference between the d.c. terminals of the bridge will be small so that very little voltage appears in reverse across the other thyristor CSR_1. If the line terminal is negative when S_A is closed exactly the same conditions exist except that the role of the diode and thyristor pairs are reversed.

The input suppression circuit L_1, R_1, C_1 will reduce the rate of rise of voltage across the a.c. terminals of the bridge as already described. The rate of rise of voltage applied to the thyristors will now be further reduced by the combined effects of the series impedance of the bridge diode and load as a series element and C_2, R_3 or C_3, R_4 as a shunt element.

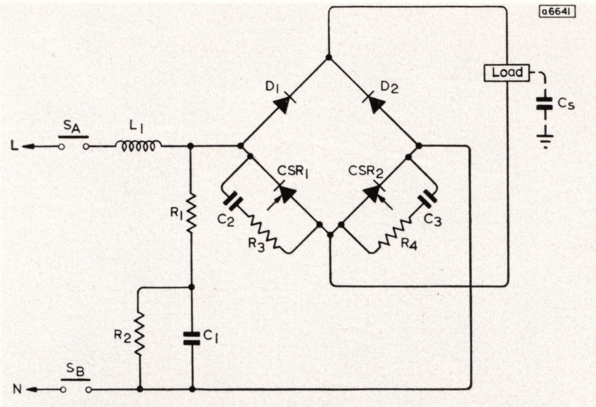


Fig. 19—Individual device suppression circuit

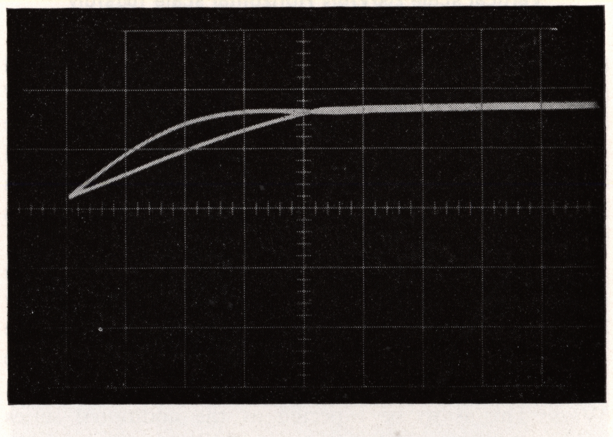


Fig. 20—Observed dV/dt in single phase bridge
Upper trace: voltage rise across a.c. terminals of bridge
Lower trace: voltage rise across thyristor
Vertical scale 200V/div Horizontal scale 20μs/div
For suppression components see text

The non-linear characteristic of the bridge diodes as a part of this second filter modifies the voltage rise characteristic across the thyristors, making the rate of rise of voltage more nearly linear as shown in Fig. 20. The upper line shows the almost exponential voltage waveform across the bridge a.c. terminals, while the lower line shows the rate of rise of voltage across the thyristor itself to be very nearly linear. In this case the component values were as follows:

$$L_1 = 160\mu H;\ C_1 = 4\mu F;\ R_1 = 5{\cdot}6\Omega.$$
$$C_2 = C_3 = 0{\cdot}22\mu F;\ R_3 = R_4 = 10\Omega.$$

It will be seen that the initial rate of rise of voltage with input suppression only is about 7·5V/μs, while with additional device suppression it is about 4·0V/μs, an improvement of nearly 2:1. Apart from the additional protection provided by individual device suppression when using double pole switching, a significant improvement is obtained in normal operation which would otherwise require a fourfold increase in either the input choke inductance or capacitance value.

With the neutral open circuit but with the circuit otherwise unchanged, the maximum rate of rise of voltage

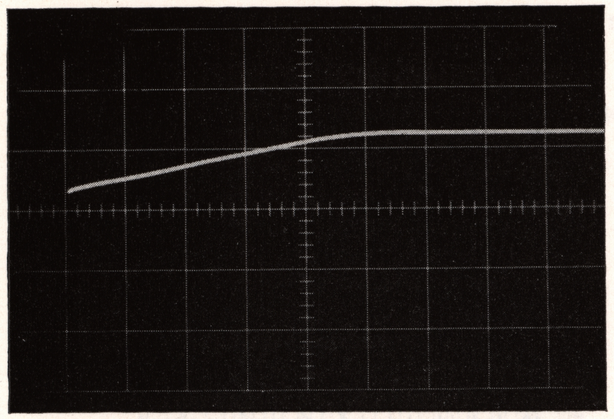


Fig. 21—Observed dV/dt in single phase bridge (as in Fig. 20 but with open circuit neutral)
Vertical scale 200V/div Horizontal scale 10μs/div

across a thyristor is as shown in Fig. 21 where the vertical scale is 200V/division and the horizontal scale 10μs/division, giving a dV/dt = 4·5V/μs. It is interesting to note that the maximum voltage reached with the neutral open circuit is only about 250V compared with the 340V shown in Fig. 20, because of the additional voltage drop across the impedance to earth.

The rate of rise of voltage across the thyristors with individual suppression and an open circuit neutral is very little affected by the series line choke. Removing the choke altogether and leaving only about 50μH of series line inductance only increases the dV/dt value to about 5V/μs. This is to be expected as the additional series impedance provided by diodes and load is considerably greater than that of the series choke.

Individual thyristor suppression is shown applied to a three phase bridge in Fig. 18. The circuit functions in the same way as the single phase system.

Peak Current in Suppression Capacitor Circuit

When the mains circuit is made, the suppression capacitors C_2 and C_3 (Fig. 19) will charge through the series line choke L_1, their individual damping resistors R_3 and R_4, and the load circuit. The peak charging current will be limited by all these series circuit elements to a moderate value, even when the mains circuit is made near the crest voltage of the supply.

When a thyristor is triggered, however, the only impedance in the capacitor discharge circuit is that of the series resistor and the thyristor itself. To avoid damaging the thyristor during its turn-on interval the rate of rise of current must be kept within the rated maximum value. The worst case will exist when the thyristor is triggered at the mid point of the cycle, at which time the suppression capacitor will be charged to its maximum voltage.

Under these conditions, measurements show that the peak discharge current is about 18A for a circuit where $C = 0{\cdot}22\mu$F, $R = 10\Omega$, and the supply voltage is 240V. The mean power dissipation in the series resistors R_3 and R_4 under these conditions is about 0·4W. A 0·5W carbon resistor was used for these measurements.

In the three phase case (Fig. 18) where the peak voltage across each thyristor is increased by a factor of $\sqrt{3}$, the peak current will be increased in the same ratio to about 30A. The resistor mean power dissipation will be increased by a factor of 3 to about 1·2W. In both cases the pulse of current is of roughly triangular shape with a duration of less than 10μs and will be within the permitted rating of most thyristors.

TRANSIENTS PRODUCED BY CONTACTORS

Magnetically operated mechanical power contactors are far from being perfect switches; they all suffer from contact surface imperfections and contact bounce effects to some extent, although some types will obviously be superior to others. It is not the intention here to discuss the characteristics of particular contactors, but rather to indicate the nature of the problem and the electrical effects which may be produced by some contactors. It should be remembered that it is not the near ideal operation of a new contactor with which we are concerned, but the operation of an old contactor in need of service but still functioning well enough to have escaped the attention of the works maintenance electrician.

To obtain some qualitative measure of the effects of contactor operation, transient voltage waveform measurements were made across a thyristor in a half controlled bridge circuit. The individual device suppression components were omitted, but the input transient suppression components were retained. So as not to confuse the results by double contact operation the neutral was left open circuit.

Fig. 22 shows typical contact bounce effects with higher frequency transients before and after each major bounce period. The vertical scale was 200V/division, the horizontal scale 1ms/division.

If one of the major bounce periods is expanded we obtain a picture like that of Fig. 23 where the time scale is now 50μs/division. The early part of this waveform may be expanded still further, when it appears as shown in Fig. 24 with a time scale of 20μs/division.

Examination of the leading edge of a single transient reveals that the rate of rise of voltage is of the order of 1000V/μs, as shown in the greatly expanded waveform of Fig. 25. Here the vertical scale has been reduced in sensitivity to 400V/division and the horizontal scale is 0·5μs/division (representing the limit of writing speed of the storage oscilloscope which was used).

It will be appreciated that repetitive transients of this type represent a serious hazard to the correct operation of thyristor equipment, and should be reduced to more reasonable proportions by suitable filters.

Fortunately, the addition of a simple RC filter across each thyristor as described on page 46 and shown in Fig. 19 provides an adequate solution. The waveform of Fig. 26 (1ms/division) should be compared with Fig. 22. It shows the effect of the additional filter components. A rather larger value of capacitance or a larger discharge resistance value gives even better results as shown in Fig. 27 (500μs/div). The main discharge path for the capacitance C_2, C_3 in Fig. 19 is R_3, the discharge resistor for the main transient suppression capacitor.

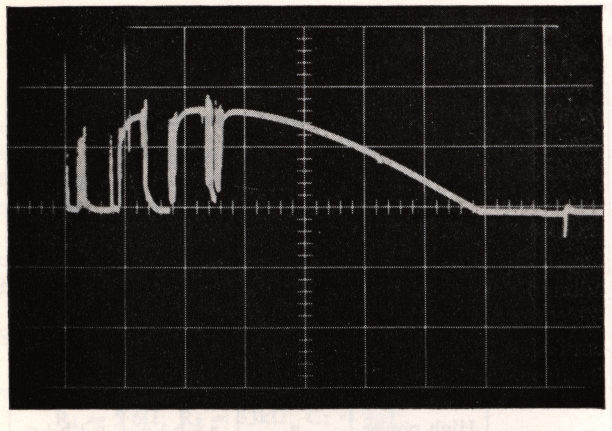


Fig. 22—Contact bounce effects with higher frequency transients before and after each major bounce period
Vertical scale 200V/div Horizontal scale 1ms/div

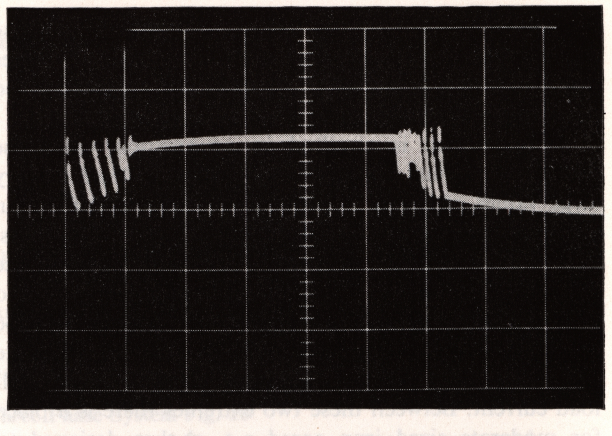


Fig. 23—Expansion of major bounce period (Fig. 22)
Vertical scale 200V/div Horizontal scale 50μs/div

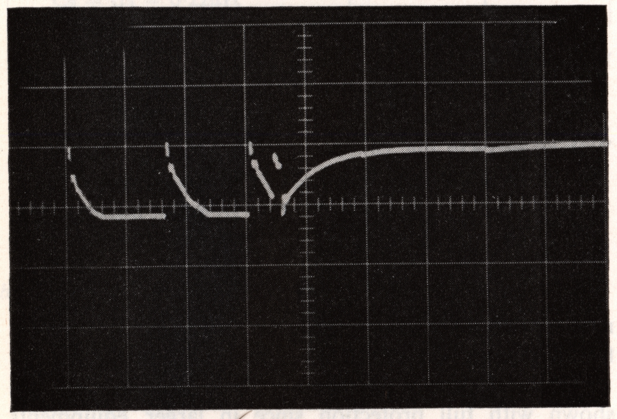


Fig. 24—Early part of Fig. 23 waveform
Vertical scale 200V/div Horizontal scale 20μs/div

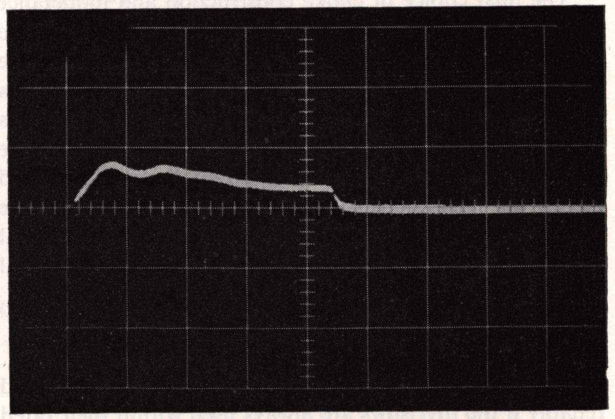


Fig. 25—Leading edge of single transient (Fig. 24)
Vertical scale 400V/div Horizontal scale 0·5μs/div

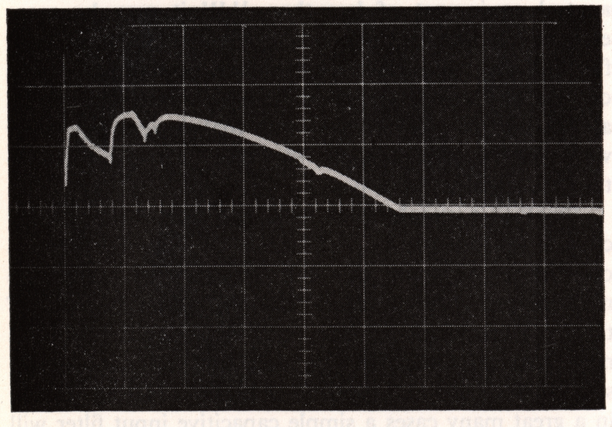


Fig. 26—Contact bounce effects with RC filter across each thyristor
(Compare with Fig. 22, which has the same scales)
Vertical scale 200V/div Horizontal scale 1ms/div

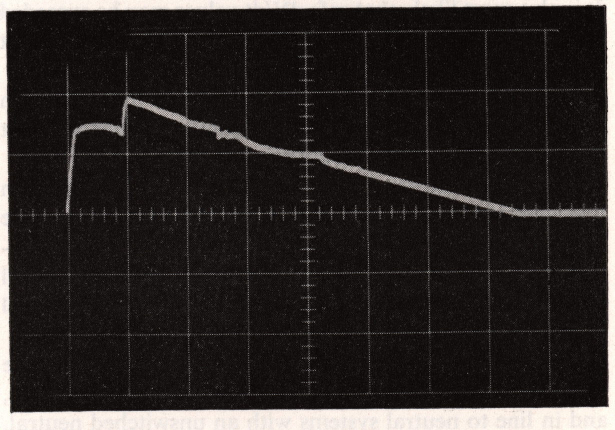


Fig. 27—Contact bounce effects as in Fig. 26 but with improved suppression circuit
Vertical scale 200V/div Horizontal scale 500μs/div

If $R_3 = 33k\Omega$ and $C_2 = C_3 = 0{\cdot}22\mu$F, the discharge time constant = 7ms. This corresponds approximately with the constants of the circuit used to obtain the waveform of Fig. 27. The maximum rate of rise of voltage in this case was about 5V/μs as described in the last section.

SERIES LINE CHOKES

The use of series chokes has already been referred to in connection with the reduction of voltage transients and dV/dt, and some indications have been given of the effects of choke Q factor. A series choke may also be used to limit peak prospective fault currents to assist in the fuse protection of thyristors and rectifiers. The design of chokes will depend very much upon whether the choke is required to perform all or only some of these functions.

If the choke is required in conjunction with fuse protection it must retain its designed inductance to very large values of current, and for this reason is usually an air cored component of quite large physical dimensions. On the other hand if the choke is only required to reduce dV/dt across non-conducting thyristors, the current up to which the design inductance must be maintained may be quite small, and ferrite cored chokes may be adequate provided that the windings are capable of carrying the full load current. Between these two extremes there is a place for moderate sized iron cored a.c. chokes designed to retain their inductance at normal load currents and so provide full transient and dV/dt protection but only partial fault current limitation.

The final choice of choke construction and inductance will depend upon a number of factors such as the degree of transient and fuse protection required, and the size and cost of the equipment, which will in turn have a bearing upon the space available for suppression chokes and the proportion of the overall cost which can be allocated for protection equipment. All these factors and others will have to be weighed up by the designer of the equipment, who will know the seriousness of an occasional device forward breakover or in the worst case an occasional device failure.

RECOMMENDATIONS

Thyristor power control circuits can only be operated reliably if the thyristors are always used within their rated peak voltages and currents and if the applied dV/dt and dI/dt values are kept within safe limits.

The magnitudes of likely mains transients are such that some suppression will be necessary in nearly all cases. It is also most likely that safe dV/dt values may be exceeded during mains switching, and this hazard may or may not be effectively reduced by a simple input filter.

In addition to its effect upon voltage transients, an input choke may be required to limit prospective fault currents to within the permitted fuse ratings.

Because of the very wide range of applications to which thyristor bridges may be put, it is very difficult to give specific recommendations on the use of suppression components. It is, however, possible to give some general guidance as to what may be required in certain general groups of equipment (see Table 1).

In most low power single phase applications it will be difficult to justify the additional cost of a series choke, and in line to neutral systems with an unswitched neutral, protection system (a) will normally suffice. In all cases of double pole switching, in particular line to line systems, components (c) must be added if the occasional forward breakover through exceeding rated dV/dt is to be avoided. Normally this will only be of any consequence when the load impedance is very low as with shunt motors, so may be omitted in low power low cost equipments.

A series choke should be used with high power resistive loads to limit dI/dt during switch-on, and with high power motor loads to limit peak prospective fault currents for fusing and to give better voltage transient protection.

TABLE 1

Recommended Suppression Systems

Load		**Suppression System**		
		Single Phase		**Three phase**
		Line to neutral	Line to line	
Resistive	Low power	a	a	—
	High power	a+b	a+b+c	a+b+c
Inductive	Low power	a	a	—
	High power	a	a+b+c	a+b+c
Motor	Low power	a	a+c	—
	High power	a+b	a+b+c	a+b+c

With reference to Fig. 19 (single phase)
$a = C_1, R_1, R_2$.
$b = L_1$
$c = C_2, R_3; C_3, R_4$

With reference to Fig. 18 (three phase)
$a = C_1, R_1, R_4; C_2, R_2, R_5; C_3, R_3, R_6$
$b = L_1; L_2; L_3$
$c = R_7, C_4 : R_8, C_5 : R_9, C_6$

All high-power line to line and three phase systems are shown with full protection since in larger equipments it is probably unwise to economise on protective components which only constitute a relatively small proportion of the overall equipment cost.

In the case of very low power single phase line to neutral equipment of less than ½kW it may be more economic to rate the thyristors to withstand the occasional full half cycle maximum load current and to accept the occasional forward breakover due to voltage transients and high dV/dt, in the knowledge that devices can safely withstand this condition, provided that the load can absorb the occasional burst of power.

Finally, it should be emphasised that we are only considering transient phenomena of largely random occurrence. At some sites the frequency of occurrence may be many times higher than in others because of the local generation of transients. Although a few cases may require particular attention and all suppression systems will have to be used to obtain satisfactory results, in a great many cases a simple capacitive input filter will suffice.

High values of dV/dt will usually only be produced when the mains contactor is operated, and then only when the contactor is operated at particular parts of the mains cycle. In the case of equipment which is run for long periods between contactor operation there will be little trouble. If, however, a motor, for example, is to be frequently started and stopped by operating the mains contactor, full suppression is recommended.

APPENDIX 1

Measurements on Practical Circuits

Measurements have been made on actual thyristor control equipments with different combinations of suppression circuits, in order to find the practical maximum value of dV/dt to the 63·2% level in each case when the input mains contactor was operated.

In all cases the input and individual thyristor suppression circuits where used, and their component values, refer to Fig. 18 and 19. The results are listed below.

Single Phase System Fig. 19

In all the single phase circuits the following component values were used:

$R_1 = 5{\cdot}6\Omega$; $R_2 = 33\text{k}\Omega$; $C_1 = 4\mu\text{F}$.
$R_3 = R_4 = 10\Omega$.

a) Line to Neutral Supply

1) L_1 = supply inductance only, approx. 50μH.
$C_2 = C_3 = 0{\cdot}22\mu\text{F}$.
S_A closed before S_B (o/c Neutral).
dV/dt = 4·7V/μs.

2) As above but $L_1 = 380\mu\text{H}$.
dV/dt = 4·7V/μs.

3) As above but $L_1 = 580\mu\text{H}$.
dV/dt = 4·4V/μs.

4) $L_1 = 380\mu\text{H}$; $C_2 = C_3 = 0{\cdot}22\mu\text{F}$.
S_B closed before S_A (solid Neutral).
dV/dt = 3·0V/μs.

b) Line to line via Auto Transformer to 240V

L_1 = leakage inductance of transformer only ≃ 1mH.
$C_2 = C_3 = 0{\cdot}22\mu\text{F}$.
S_A closed before S_B.
dV/dt = 4·3V/μs.

c) Line to Line via Double Wound Transformer to 240V

L_1 = leakage inductance of transformer only ≃ 2mH.
$C_2 = C_3 = 0{\cdot}22\mu\text{F}$.
S_A closed before S_B.
dV/dt = 4·0V/μs.

d) Line to Neutral Supply

Effect on dV/dt of value of C_2 and C_3 with all other component values constant.

$C_2 = C_3 =$	0	0·05	0·1	0·22	μF
dV/dt =	12·5	7·7	5·8	3·7	V/μs

Three Phase System Fig. 18

In all cases the following component values were used:

$R_1 = R_2 = R_3 = 5{\cdot}6\Omega$
$R_4 = R_5 = R_6 = 33\text{k}\Omega$
$R_7 = R_8 = R_9 = 10\Omega$
$C_1 = C_2 = C_3 = 4\mu\text{F}$
$L_1 = L_2 = L_3 \simeq 2\text{mH}$

a) $C_4 = C_5 = C_6 = 0{\cdot}025\mu\text{F}$
Input suppression returned to neutral
dV/dt = 4V/μs.

b) As above but $C_4 = C_5 = C_6 = 0{\cdot}22\mu\text{F}$
dV/dt = 2·9V/μs

c) $C_4 = C_5 = C_6 = 0{\cdot}22\mu\text{F}$
Input suppression connected as in Fig. 18
dV/dt = 3·5V/μs

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1. NOLF, J. M., Applications Thyristors VIII: Evaluation du circuit RC optimal limitant la croissance de tension aux bornes de thyristors bloques. To be published in Revue M.B.L.E. (in French) by M.B.L.E. Brussels.

Junction Field Effect Transistors: their Structure and Operation

B. J. M. OVERGOOR
Semiconductor Application Laboratory, Philips, Nijmegen

The structure and operation of junction field effect transistors are briefly described, particular attention being given to those of the n-channel depletion mode type. Frequency-dependent and frequency-independent properties of such a transistor are then discussed with reference to pertinent equations and graphs. Finally, the noise properties are considered in terms of an equivalent fourpole.

INTRODUCTION

The junction field effect transistor has properties that enable it both to outperform conventional transistors in some of their established applications, and to fill some roles for which conventional transistors are completely unsuitable. Having been patented* as long ago as 1928, it can hardly be called new; however, its impact on practical electronics had to await the development of advanced solid-state technology and is therefore quite recent. This article describes the general characteristics and structure of such a transistor.

MODE OF OPERATION

Typically, a junction field effect transistor consists of a conducting channel enclosed for part of its length by a p-n junction, as shown in simplified form in Fig. 1. One end of the channel is called the source (S), the other end the drain (D), and the enclosing material that forms the junction the gate (G); these can be compared with the cathode, anode, and grid respectively, of an electron tube.

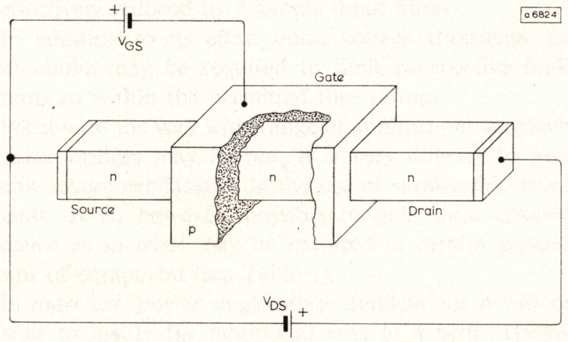

Fig. 1—Schematic representation of a junction field effect transistor

If the channel is of n-type material and the gate of p-type, as in Fig. 1, the transistor is called an n-channel device; if the opposite arrangement is used, a p-channel device.

The usefulness of a field effect transistor is based on the ability of the gate-source potential to control the conductance of the channel, and hence the current flow between source and drain. Application of a reverse bias V_{GS} across the p-n junction (Fig. 2) creates a space charge which partly depletes the channel of carriers and reduces its conductance; the bias value at which the conductance falls to zero is known as the pinch-off voltage V_P.

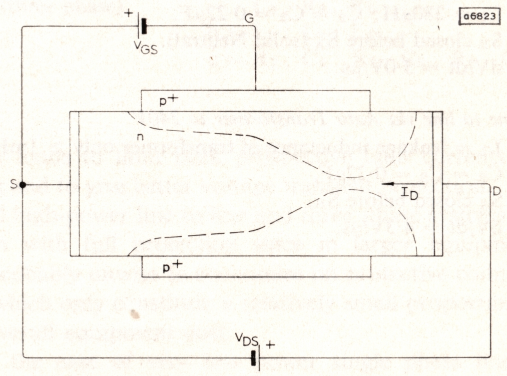

Fig. 2—Cross-section of a junction field effect transistor, showing the depletion zone in the channel (schematic)

The current I_D which flows through the channel at given values of V_{GS} and V_{DS} occasions a voltage gradient in the channel such that the depletion zone gradually widens as the drain is approached (Fig. 2). Since the current density at the drain exceeds that at the source, the field strength near the drain also exceeds that near the source. Beyond a certain value of the drain voltage, satisfying the condition:

$$V_{DG} = V_{DS} - V_{GS} > -V_P\,,$$

the depletion zone will constrict the channel at the drain, very nearly cutting it off; very nearly, but not completely, because the current which is already flowing must be passed. At the constriction the field strength will have become so large that the mobility of the electrons starts to diminish (they approach their greatest drift velocity). Any further increase of the drain voltage will not raise the drain current to any great extent.

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*U.S. patent 1 900 018 was granted to Lilienfeld for a 'device for controlling electric current'.

CONSTRUCTIONAL DETAILS

The structure of the junction field effect transistors BFW10 and BFW11 is shown schematically in Fig. 3. A high-conductivity substrate of p-type silicon, which acts as the gate, is provided with an n-type epitaxial layer. Into this layer p^+ type diffusions I and II are made; the former penetrate into the p-type substrate, so that an n-type island of special shape, the channel, is obtained.

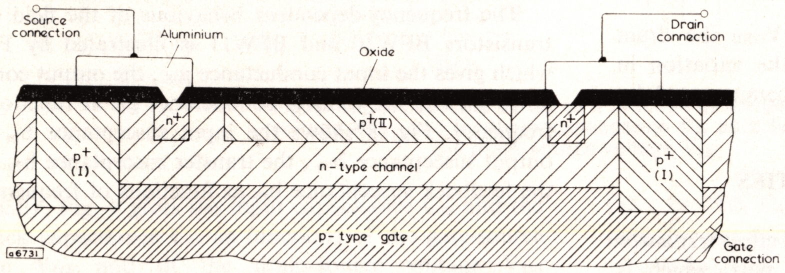


Fig. 3—Structure of a junction field effect transistor

In practice, several channels are interdigitated and connected in parallel to provide a high transconductance. The last diffusion step produces n^+ regions in the channel to diminish the series resistances to the source and drain connections and to ensure good contacts. On these n^+ regions aluminium bonds are deposited to which the source and drain contact wires are fixed, thus ensuring reliable contact.

FREQUENCY-INDEPENDENT PROPERTIES

Current versus Voltage Characteristics

The typical characteristic of an n-channel junction field effect transistor will be explained with reference to Fig. 4. The relation between the drain current I_D and the drain-source voltage V_{DS}, with the gate-source voltage V_{GS} as parameter, is shown in Fig. 5. The plane is divided into two regions by the curve (shown by the broken line):

$$V_{DS} = V_{GS} - V_P\,.$$

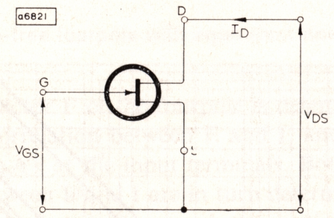


Fig. 4—Symbol of a field effect transistor and the denomination of its terminals

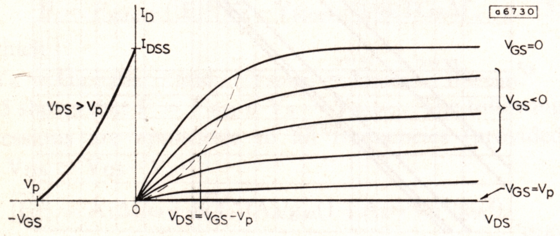


Fig. 5—Characteristics of a field effect transistor, representing the drain current I_D as a function of the gate-source voltage V_{GS} and of the drain-source voltage V_{DS}, with V_{GS} as parameter

To the right of the curve is the so-called pinch-off region in which the output conductance is much lower than to the left. At a constant drain-source voltage, the drain current in the pinch-off region obeys the equation:

$$I_D = I_{DSS}(1 - V_{GS}/V_P)^n, \qquad \ldots(1)$$

in which I_{DSS} denotes the drain current at $V_{GS} = 0$ and $V_{DS} > |V_P|$, and the exponent n amounts to almost 2.

Transconductance

The transconductance g_m of a field effect transistor adjusted to the pinch-off region can be found by differentiating Eq. 1. Putting $n = 2$ and assuming $V_{DS} > V_{GS} - V_P$ gives:

$$g_m = (2/V_P)(I_D I_{DSS})^{\frac{1}{2}}. \qquad \ldots(2)$$

Output Conductance

Eq. 1 suggests that the output conductance g_{os} is zero. However, I_{DSS} and n both depend slightly on V_{DS}, so, provided that $V_{DS} > V_{GS} - V_P$, the output conductance is, to a good approximation:

$$g_{os} = (2/V_0)(I_D I_{DSS})^{\frac{1}{2}}. \qquad \ldots(3)$$

The voltage V_0 is determined by the length of the channel and by the field strength at which the mobility of the electrons starts to decrease. It is usually of the order of 500V; for the BFW10 and BFW11 it ranges from 700V to 300V.

From Eqs. 2 and 3, the output conductance may also be expressed by:

$$g_{os} = g_m V_P / V_0\,.$$

Input Conductance

In comparison to bipolar transistors, junction field effect transistors have a very low input conductance, about equal to that of a reverse biased diode. For the BFW10 and BFW11 it is of the order of 10^{-10}mho (corresponding to an input resistance of 10GΩ) at room temperature, the leakage current then averaging between 50pA and 100pA.

Temperature Dependence of the Working Point

The drain current is affected by two temperature-dependent quantities that work in opposition to each other, namely:

1) the mobility of the majority carriers in the channel,

$$(1/\mu)(d\mu/dT) \simeq -1{\cdot}5/T,$$

2) the pinch-off voltage V_P, which is given by:

$$dV_p/dT = d\Phi/dT \simeq -2\text{mV/degC},$$

in which Φ is the diffusion potential of the p-n junction.

Which of the two effects will predominate depends on how the transistor is biased.

To keep the drain current constant, the gate voltage should change with temperature at a rate:

$$\frac{dV_{GS}}{dT} = -\frac{1}{\mu}.\frac{d\mu}{dT}.\frac{1}{n}(V_{GS}-V_p)+\frac{dV_P}{dT}, \qquad \ldots(4)$$

in which $n \simeq 2$ (cf. Eq. 1). From Eq. 4 it follows that the gate voltage V_{GSo} at which $dV_{GS}/dT = 0$ amounts to

$$V_{GSo} \simeq V_p+0{\cdot}7V.$$

If the gate-source voltage is equal to V_{GSo} the drain current is independent of temperature, the variation in mobility of the majority carriers being compensated by the change of the pinch-off voltage.

FREQUENCY-DEPENDENT PROPERTIES

Input Admittance

The input admittance of a junction field effect transistor increases with frequency. Its imaginary part, which is almost proportional to frequency, is due to the space charge capacitance C_{gc} of the reverse biased gate-to-channel diode close to the source, and to the capacitance C_{gb} of the overlap between one of the contact bonds of the source and the diffused isolation layer (Fig. 6). The total gate-to-source capacitance is approximately:

$$C_{gs} = C_{gb}+C_{gc} \simeq 3pF.$$

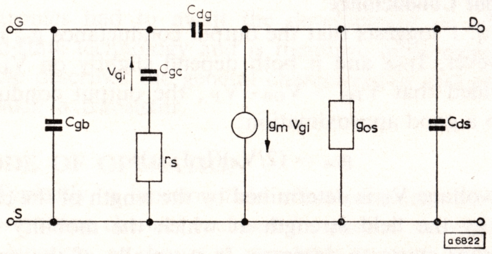


Fig. 6—Equivalent circuit of a junction field effect transistor

The space charge contributes a much greater part to the input capacitance than to the feedback capacitance. This is because the width of the space charge region facing the source, and contributing to the input capacitance, is much smaller than the space charge region that faces the drain and contributes to the feedback capacitance (Fig. 2).

Part of the channel between the source and the constriction forms a resistance r_s in series with the input capacitance. This series resistance, which causes the real part of the input admittance to rise with the square of the frequency, can be approximated by $r_s = 1/3g_m$.

Transfer Admittance

The intrinsic transconductance g_m of junction field effect transistors remains constant up to very high frequencies (about 900MHz), the transit time of the electrons travelling from source to drain being very short.

As a result of the feedback capacitance C_{gd} (Fig. 6), the externally measured transfer admittance y_{fs} has an imaginary component. The feedback capacitance C_{gd} is due to the space charge of the reverse biased gate-to-channel diode near the drain and to the overlap between the aluminium contact bonds of the drain and the diffused isolation layer which is at the same potential as the gate. Together, these make up a total feedback capacitance of about 0·5pF (including the capacitance caused by the envelope).

The real part of the measured transfer admittance is reduced to some extent by the internal input resistance r_s (see above).

Characteristics

The frequency-dependent behaviour of the field effect transistors BFW10 and BFW11 is illustrated by Fig. 7 which gives the input conductance g_{is}, the output conductance g_{os} and the transfer conductance g_{fs} as functions of frequency. Fig. 8 shows the input susceptance b_{is}, the output susceptance b_{os}, the transfer susceptance b_{fs}, and the feedback susceptance b_{rs} as functions of frequency.

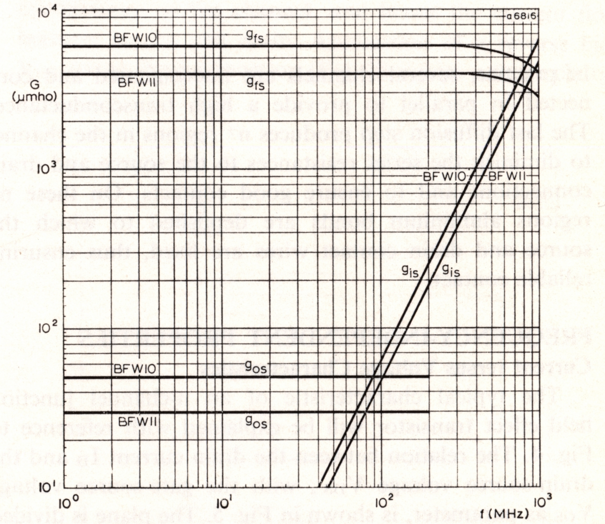


Fig. 7—Input conductance g_{is}, output conductance g_{os} and transfer conductance g_{fs} of transistors BFW10 and BFW11 as functions of frequency f

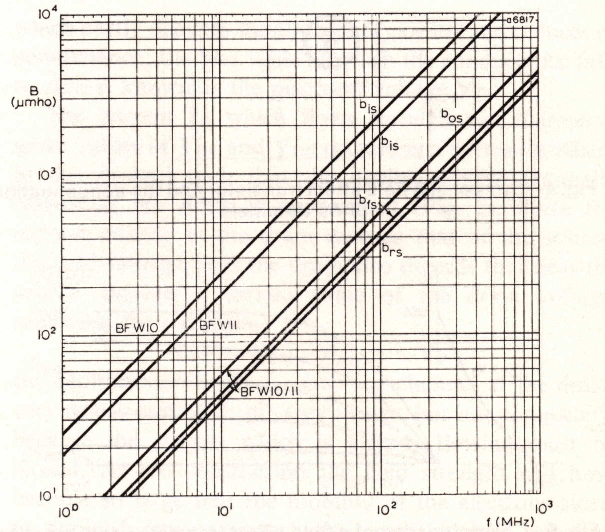


Fig. 8—Input susceptance b_{is}, output susceptance b_{os}, transfer susceptance b_{fs} and feedback susceptance b_{rs} of transistors BFW10 and BFW11 as functions of frequency f

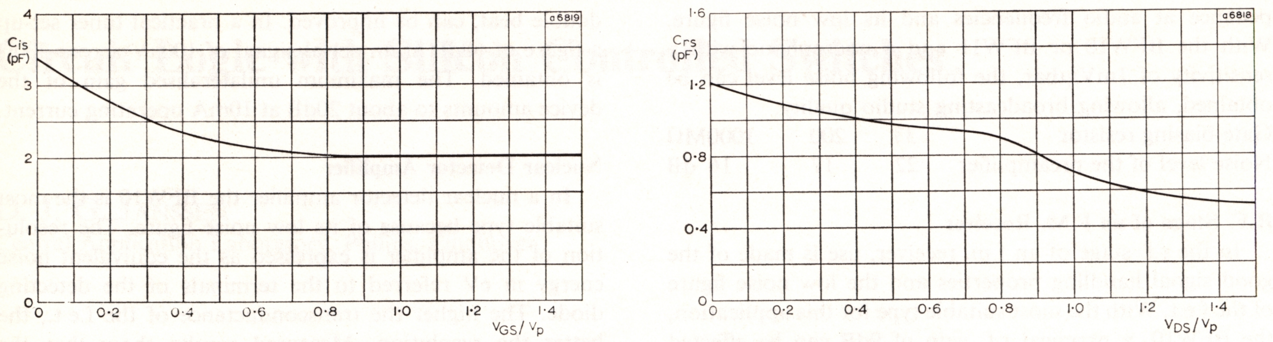


Fig. 9—Input capacitance C_{is} as a function of the gate-source voltage V_{GS}, and feedback capacitance C_{rs} as a function of the drain-source voltage V_{DS}

Finally, Fig. 9 gives the input capacitance C_{is} and the feedback capacitance C_{rs} as functions of the gate-source voltage V_{GS} and of the drain-source voltage V_{DS} respectively.

Noise

The noise in junction field effect transistors is distinguishable into two types:

1) thermal noise (and the so-called excess noise for audio frequencies) which is due to fluctuations in the conductance of the channel,
2) shot noise due to the gate-to-channel diode.

The noise may be represented by an equivalent voltage source E and an equivalent current source I at the input terminals of a fourpole which is itself assumed to be noise-free, as shown in Fig. 10.

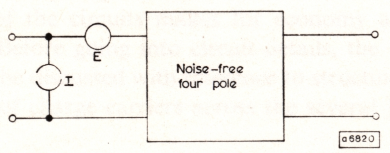


Fig. 10—Noise-free fourpole with equivalent noise sources

The noise factor F of the fourpole is determined by E, by I, by the correlation between E and I, and finally by the admittance Y_S at the input terminals. Both I and the correlation between E and I are in turn determined by the minimum noise factor F_{min} and the optimum source admittance $Y_{S(opt)}$. The noise factor may be calculated from the expression:

$$F = F_{min}+(\overline{|E|^2}|Y_S-Y_{S(opt)}|^2)/4kTG_S\Delta f, \quad \ldots(5)$$

in which

$$Y_S = G_S+jB_S \quad \text{and} \quad Y_{S(opt)} = G_{S(opt)}+jB_{S(opt)}.$$

Eq. 5 shows that $F = F_{min}$ if $Y_S = Y_{S(opt)}$. The following expressions are applicable to all frequencies (provided that $V_{DS} > V_{GS}-V_P$):

$$\overline{|E|^2} = A_1\Delta f/\omega+4kT\Delta fA_3/g_m(1+A_2\omega^2C_g{}^2/g_m{}^2), \quad \ldots(6)$$

and

$$\overline{|I|^2} = 2qI_G\Delta f+4kT\Delta fA_4\omega^2C_g{}^2/g_m. \quad \ldots(7)$$

In these expressions q denotes the electron charge (16×10^{-20}C), C_g the total input capacitance, and I_G the gate leakage current, whilst

$$A_1 \simeq 10^{-13}\,(I_{DSS}/I_D)^{\frac{1}{3}} \qquad A_3 \simeq 0{\cdot}7$$
$$A_2 \simeq 0{\cdot}11 \qquad A_4 \simeq 0{\cdot}6$$

For the 'white' and r.f. noise range it is further permissible to put:

$$F_{min} \simeq 1+0{\cdot}8\omega C_{gc}/g_m+0{\cdot}3\omega^2C_{gc}{}^2g_m{}^2,$$
$$B_{S(opt)} \simeq -0{\cdot}8\omega C_{gc}-\omega C_{gb}-\omega C_{gd} \simeq -\omega C_{is},$$
$$G_{S(opt)} \simeq 0{\cdot}6\omega C_{gc}.$$

T is temperature in degrees Kelvin, k is Boltzmann's constant.

TYPICAL APPLICATIONS

The following notes outline several types of application in which the junction field affect transistor may be used. The figures quoted are intended as indications of the performances that may be expected. Detailed applications information will be made available later.

Preamplifier of a Wideband Oscilloscope

With the BFW10 in the front end of an oscilloscope preamplifier, and two stages equipped with the BFY90, the following properties can be obtained:

Input impedance	1MΩ (parallel capacitance 7·5pF)
Rise time	<1ns
Noise voltage	<0·5mV peak-to-peak (referred to the input)
Voltage drift with temperature	<0·2mV/degC (referred to the input).

These properties are sufficiently good for designing oscilloscopes with an input sensitivity of 5mV/cm and a bandwidth of up to 150MHz.

D.C. Amplifier with very small Current Drift

With the BFW10 or BFW11 used in the differential input stage of a d.c. amplifier a very small current drift (about 1pA/degC, referred to the input of the amplifier) can be realised. In spite of the relatively large voltage drift (10 to 100μV/degC, depending on the gate voltage) very good d.c. amplifiers can be made for source impedances higher than several megohms.

Capacitor-microphone Preamplifier

The f.e.t. is eminently suited for use in a capacitor-microphone preamplifier, because of its high input impedance at audio frequencies and its low noise figure. With the BFW10 or BFW11 and a microphone with a sensitivity of 1mV/μbar, the following noise level can be obtained, allowing broadcasting studio quality.

Gate-biasing resistor	33	200	1000MΩ
Noise level of the preamplifier	22	17	16 dB

R.F. Stage of an F.M. Receiver

In the r.f. stage of an f.m. receiver, use is made of the good signal handling properties and the low noise figure of the f.e.t. With the most suitable type for this application, the BFW10, a practical r.f. gain of 9dB can be effected without neutralisation, and the r.f. stage is stable even without the aerial connected. A noise figure of better than 3·5dB can be obtained. Also, the suppression of harmonics-interference effects, such as repeat spot and double beat, can be improved. In a practical tuner set-up a figure of 60dB at an aerial signal of 100μV across 300Ω is obtained. The maximum unilateralised gain of the device amounts to about 20dB at 10mA operating current.

Nuclear Detector Amplifier

In a nuclear detector amplifier the BFW10 is the most suitable type because of its low noise figure. The resolution of the amplifier is expressed as the equivalent noise energy in eV referred to the terminals of the detecting diode. The higher the transconductance of the f.e.t., the better the resolution. Measured results show that the BFW10, having a minimum transconductance of 3·2mmho, gives a resolution of 0·7 to 0·9keV if the input is not terminated by a capacitor. A rate of change in resolution of approximately 50 to 60eV/pF has also been measured.

Circuit Logic with Silicon Controlled Switches

D. J. G. Janssen
Central Application Laboratory, Philips, Eindhoven

Equations governing the movement of charge carriers in the p-n-p-n structure of a silicon controlled switch are given and its electrical behaviour is described, comparisons being drawn with the operation of more familiar semiconductor devices such as thyristors and transistors.

To illustrate the wide range of applications of the silicon controlled switch, a number of circuits are described; these include ring counters, driving circuits for numerical indicator tubes and print-out devices, and several gate circuits.

INTRODUCTION

A silicon controlled switch, of which the BRY39 is a typical example, is a p-n-p-n semiconductor device that structurally resembles a small thyristor, except that all four electrodes are accessible. Functionally it is comparable to a low-power transistor combined with a holding circuit. As will be shown, the interaction and accessibility of the four electrodes open new and advantageous ways to the performance of many switching and logic operations for which two or more active elements would otherwise be needed. Fairly large currents can be switched, and the simplicity of the circuits makes for economy as well as reliability. Before going into circuit details, the operating theory will be discussed with reference to structure and the movement of charge carriers across the several junctions.

STRUCTURE

Fig. 1 shows the conventional symbol for the silicon controlled switch and its internal 'circuit'. The illustration of the symbol indicates alternative names for the four electrodes. Fig. 2 shows the internal structure of the device.

The s.c.s. can be considered as two transistors: first, an n-p-n transistor (TR_1 in Fig. 1), and second, a p-n-p transistor (TR_2 in Fig. 1). In Fig. 2, the two transistors are represented by:

	TR_1 (n-p-n)	TR_2 (p-n-p)	
		A	Emitter
Collector	C	C	Base
Base	B	B	Collector
Emitter	E		

In the following discussion the terms emitter, base, collector, and anode (as shown in Fig. 3) will be used.

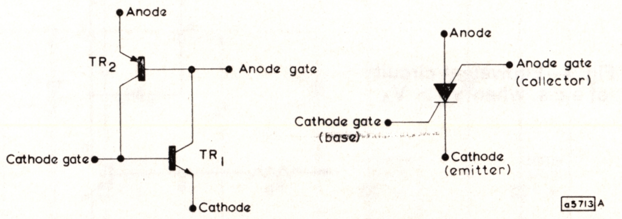
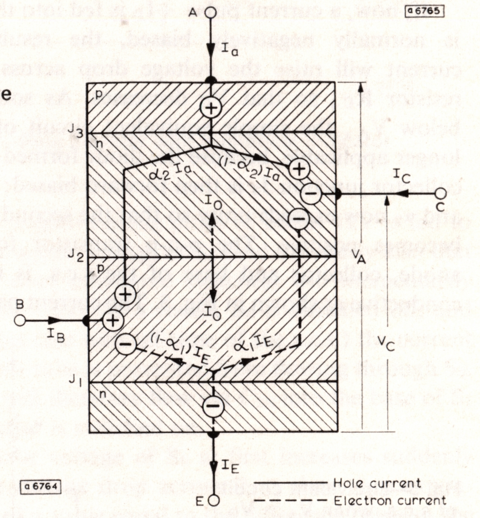


Fig. 1—Silicon controlled switch internal 'circuit' and conventional symbol

Fig. 2—Structure of s.c.s.



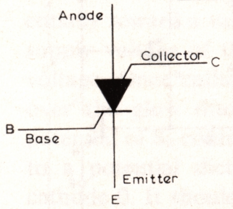


Fig. 3—Electrode terminology used in the present article

THEORY OF OPERATION

Two steady states are possible, and in both equilibrium is maintained by a leakage current across the common junction J_2 (Fig. 2). Moreover, a fraction $\alpha_1 I_E$ of the emitter current and a fraction $\alpha_2 I_A$ of the anode current flow through this junction, α_1 and α_2 being respectively functions of the currents through the n-p-n and the p-n-p transistors.

In the base region of the n-p-n transistor the equation

$$(1-\alpha_1)I_E = \alpha_2 I_A + I_B + I_0\,, \qquad \ldots(1)$$

and in the collector region the equation

$$(1-\alpha_2)I_A = \alpha_1 I_E - I_C + I_0\,, \qquad \ldots(2)$$

describing the recombination of charge carriers, must be fulfilled. From Eqs. 1 and 2:

$$I_C = \frac{1}{1-\alpha_1}.I_0 + \frac{\alpha_1}{1-\alpha_1}.I_B + \frac{\alpha_1+\alpha_2-1}{1-\alpha_1}.I_A \qquad \ldots(3)$$

As a rule the first term is so small with respect to the others that Eq. 3 may be simplified to:

$$I_C \simeq \frac{\alpha_1}{1-\alpha_1}.I_B + \frac{\alpha_1+\alpha_2-1}{1-\alpha_1}.I_A \qquad \ldots(4)$$

So long as V_C exceeds V_A, junction J_3 is reverse-biased so that the p-n-p transistor is cut off and I_A becomes negligibly small. The second term of Eq. 4 can then be disregarded, and the s.c.s. operates as a normal n-p-n silicon planar transistor with emitter E, base B, and collector C (Fig. 4).

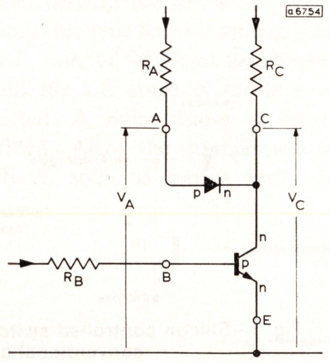


Fig. 4—Equivalent circuit of s.c.s. when $V_C > V_A$

If, now, a current pulse $+I_B$ is fed into the base, which is normally negatively biased, the resulting collector current will raise the voltage drop across the collector resistor R_C, so that V_C decreases. As soon as V_C falls below V_A, the simple equivalent circuit of Fig. 4 is no longer applicable, because the diode formed by the anode-collector junction J_3 is then forward biased; the sum of α_1 and α_2 now exceeds unity so that the second term of Eq. 4 becomes positive. The p-n-p transistor formed by the anode, collector and base of the s.c.s. is then rendered conductive as shown in Fig. 5. The current passing through this transistor flows back into the base of the n-p-n transistor, so that the original base current $+I_B$ is augmented. This raises the collector current I_C which, by virtue of the increased base current of the p-n-p transistor, leads to a further increase of the current flowing through the s.c.s. This process continues until the collector-to-emitter voltage and the anode-to-emitter voltage have reached their saturation values and the s.c.s. is in the ON state.

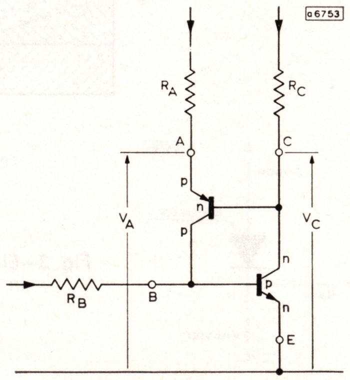


Fig. 5—Equivalent circuit of s.c.s. when $V_A > V_C$

Since the current that keeps the n-p-n transistor in the ON state is supplied by the p-n-p transistor, the s.c.s. remains in this state after the positive-going base current pulse has ceased. Eq. 4 reveals that the value of I_A which is required to keep the s.c.s. in the ON state (termed the holding current I_H) depends on the external reverse base current $-I_B$. It can be derived from this equation that the condition for keeping the s.c.s. in the ON state is:

$$I_H > \left(I_C - \frac{\alpha_1}{1-\alpha_1}.I_B\right)\left(\frac{1-\alpha_1}{\alpha_1+\alpha_2-1}\right). \qquad \ldots(5)$$

For most practical purposes the holding current of the BRY39 may be taken to be:

$$I_H > (I_C - 50I_B)/20. \qquad \ldots(6)$$

Because the ON state is maintained by the anode once a short driving pulse has been applied to the base (usually via a capacitance), an s.c.s. might be considered as a transistor incorporating a holding circuit, no continuous driving current being required to keep it in the ON state. This use of the anode as a control electrode explains why the output signal of an s.c.s. is commonly taken from the collector.

The usual procedure to return the s.c.s. to the OFF state is to reduce I_A temporarily below I_H. To this end a negative voltage is applied to the anode so that the direction of I_A is momentarily reversed. The anode-collector junction J_3 then becomes reverse-biased after about 0·1μs and the situation represented in Fig. 4 is restored. The base being negatively biased, an n-p-n transistor with reverse base current is thus obtained, which is completely cut off within a few microseconds. The sum of these two intervals is termed the 'turn-off time.'

By analogy with the procedure applied to thyristors designed for gate turn-off, it might be supposed that an alternative way to return the s.c.s. to the OFF state would be to raise the negative base current $-I_B$ until the current left for driving the n-p-n transistor became insufficient. This method is impracticable, however, because the voltage drop produced by $-I_B$ across the internal base resistance would usually exceed the permissible maximum of -5V across the base-emitter junction J_1.

There is, however, another method of switching off an s.c.s., namely by raising the collector current I_C. For practical reasons this is feasible only if a suitable resistor R_E is included in the emitter circuit, as shown in Fig. 6.

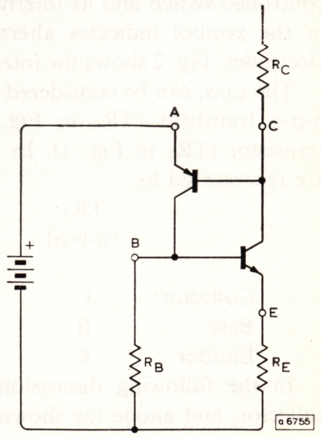


Fig. 6—Circuit in which s.c.s. can be switched off by raising I_C

So long as anode current flows, the emitter current will remain almost constant, equalling the difference between the supply voltage and the substantially constant anode-to-emitter saturation voltage, divided by the resistance R_E. The collector current can thus be increased at the expense of the anode current until the latter drops below the holding value and the s.c.s. is switched off.

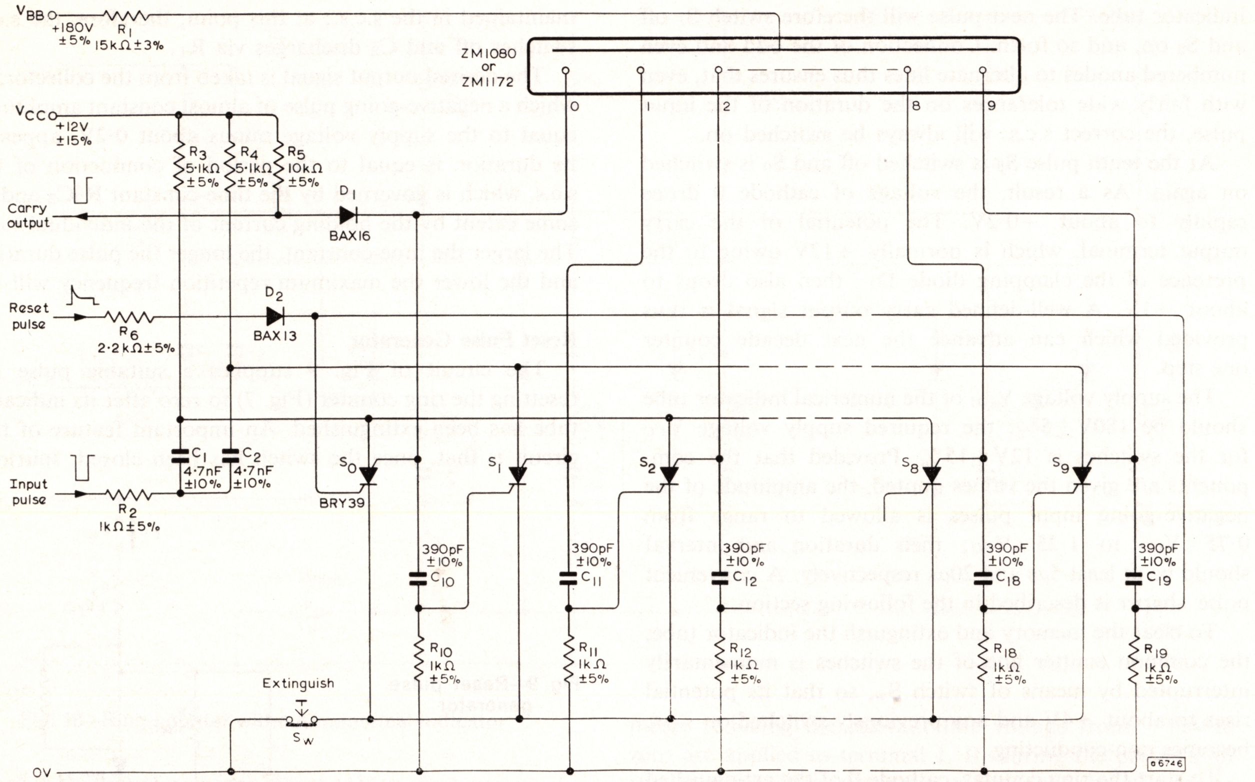


Fig. 7—Ring counter with numerical indicator

ILLUSTRATIVE CIRCUITS

A few of the many types of circuit in which the BRY39 can be used will now be discussed. In all circuits except Figs. 7 and 15 the component values shown are merely indicative, no attempt having been made to render the designs optimal. In fact, the optimum design is usually governed by external conditions which differ from case to case, such as the required speed and the expected deviations of the supply voltages and input signals from their nominal values. The circuits shown can easily be adapted to these variations.

Ring Counter with Numerical Indicator

The BRY39 makes it possible to build ring counters that are simpler and less expensive than the usual designs based on bistable multivibrators. This is clearly shown by Fig. 7, which gives the circuit diagram of one decade of such a counter. The component values have been so chosen that no stringent requirements are imposed on the amplitude and duration of the input pulses or the constancy of the supply voltages.

To explain the operation of this circuit the s.c.s. denoted by S_0 will be assumed to be in the ON state, the cathode 0 of the indicator tube being lit. The anode and collector of S_0 are then at a low potential (about +1V and +0·2V respectively), whereas the collectors of S_1 to S_9 have potentials that may range from +15V to +120V, depending on the probe currents of the relevant cathodes of the indicator tube and the s.c.s. leakage currents.

If, now, a negative-going pulse of about 12V is fed to the input, the anode voltage of S_0 (and obviously also that of the other even numbered switches) will momentarily drop to about -5V. As a result, S_0 is switched off, and after about 2μs (the turn-off time of the s.c.s.) the current of the indicator tube is prevented from flowing through S_0. This current will therefore flow via C_{10} into the base of S_1 so that the latter is switched on.

The collector voltage of S_0 at first increases suddenly owing to the voltage drop across R_{10}, then rises exponentially toward a value equal to the difference between the supply voltage of the indicator tube and its maintaining voltage. Once cathode 1 of the indicator tube has taken over the glow discharge from cathode 0, the collector potential of S_0 continues to rise, but at a much slower rate, to a potential dictated by the probe characteristics of cathode 0. It should be noted that the base-emitter diode of S_1 maintains the lower end of capacitor C_{10} almost at earth potential.

Although the input pulse also reduces the anode voltage of the odd numbered switches, this does not prevent S_1 from being switched on; the circuit has been designed so that the anodes do not at first drop below about +6V.

Once S_1 is switched on, its collector potential drops to about +0·2V and its anode potential to about +1V, as does the anode potential of the other interconnected, odd numbered switches; the anode potential of the even numbered switches, however, rises to +12V. The collectors of all switches, except the one that is switched on, again assume high positive potentials, governed by the probe characteristics of the several cathodes of the numerical indicator tube. The next pulse will therefore switch S_1 off and S_2 on, and so forth. Connection of the odd and even numbered anodes to alternate lines thus ensures that, even with fairly wide tolerances on the duration of the input pulse, the correct s.c.s. will always be switched on.

At the tenth pulse S_9 is switched off and S_0 is switched on again. As a result, the voltage of cathode 0 drops rapidly to about +0·2V. The potential of the carry output terminal, which is normally +12V owing to the presence of the clamping diode D_1, then also drops to about +1V. A well-defined carry output signal is thus provided which can advance the next decade counter one step.

The supply voltage V_{BB} of the numerical indicator tube should be 180V±5%; the required supply voltage V_{CC} for the switches is 12V±15%. Provided that the components are given the values quoted, the amplitude of the negative-going input pulses is allowed to range from $0{\cdot}75 \times V_{CC}$ to $1{\cdot}25 \times V_{CC}$; their duration and interval should be at least 5μs and 20μs respectively. A convenient pulse shaper is described in the following section.

To clear the memory and extinguish the indicator tube, the common emitter line of the switches is momentarily interrupted by means of switch S_w, so that its potential rises to about +4V and any previously switched-on s.c.s. becomes non-conducting.

To start the ring counter, cathode 0 of the extinguished indicator tube can be lit by feeding a single positive-going pulse to the reset terminal. A circuit for providing a suitable reset pulse is described later.

Pulse Shaper

Fig. 8 shows the circuit of a pulse shaper suitable for supplying input signals to the ring counter described above. A positive-going pulse fed to the base of the BRY39 gives rise to a substantially square-wave pulse of fixed amplitude and duration at the collector.

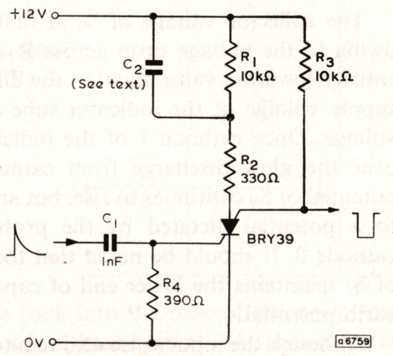


Fig. 8—Pulse shaper for driving Fig. 7 ring counter

In the quiescent condition the base is biased to the emitter potential, 0V, and the s.c.s. is switched off. In response to a positive-going pulse fed to the base via capacitor C_1, the initial bias is temporarily overcome and the s.c.s. is switched on, anode current being supplied via C_2. Since the current flow through R_1 is insufficient to maintain the s.c.s. in the switched-on condition, the period of conduction depends on the charging time of C_2. As the charge increases, the anode current decreases, eventually falling to a value at which conduction can no longer be maintained in the s.c.s.; at this point, therefore, the s.c.s. switches off and C_2 discharges via R_1.

The desired output signal is taken from the collector, at which a negative-going pulse of almost constant amplitude, equal to the supply voltage minus about 0·2V, appears; its duration is equal to the period of conduction of the s.c.s. which is governed by the time-constant R_2C_2 and to some extent by the holding current of the individual s.c.s. The larger the time-constant, the longer the pulse duration and the lower the maximum repetition frequency will be.

Reset Pulse Generator

The circuit of Fig. 9 supplies a suitable pulse for resetting the ring counter (Fig. 7) to zero after its indicator tube has been extinguished. An important feature of this circuit is that, once the switch has been closed, spurious impulses due to contact bounce have no effect; a single output pulse of fixed shape is produced, with which all decades of the counter can be reset simultaneously.

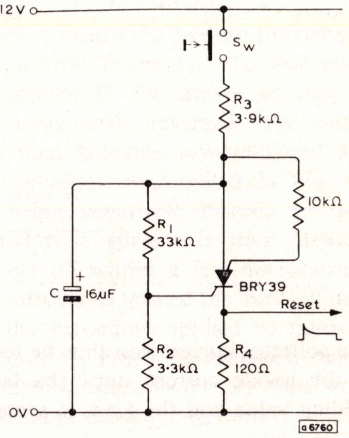


Fig. 9—Reset pulse generator

Upon closure of switch S_w, as soon as capacitor C is charged the s.c.s. is switched on by the current flowing into its base. The capacitor then rapidly discharges via the s.c.s. and its emitter resistor R_4, across which a positive-going reset pulse of the required duration is produced. This pulse subsequently decays to a very low value determined by the ratio of R_3 and R_4, and it ceases completely when the switch is released.

Ring Counter without Numerical Indicator Tube

In some cases a decade counter is required which need not display the number of pulses on a numerical indicator tube. Such a counter may, for example, be used for driving a control circuit for a numerical print-out device (see page 62). In that case the circuit of Fig. 7 may be simplified as indicated in Fig. 10.

Comparison with Fig. 7 shows that the indicator tube has been replaced by ten resistors (R_{10} to R_{19}) linked to a common supply line. To ensure that the s.c.s. collectors remain positive with respect to their anodes, even in the event of a heavy external load, this line should be connected to a +24V source; if the +12V line were used, an s.c.s. might be wrongly switched on via its internal 'p-n-p transistor'.

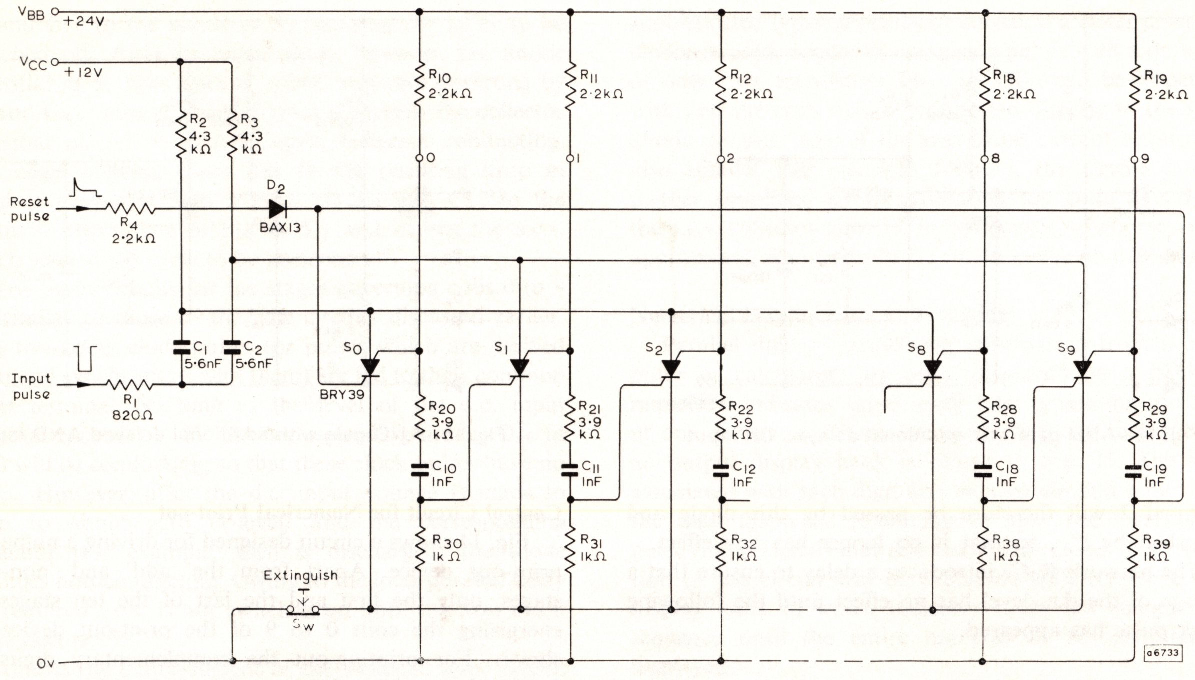


Fig. 10—Ring counter without numerical indicator

Negative-going pulses can be taken from the terminal points 0, 1, 2, ... , 8 and 9. To limit the amplitude at any of the terminal points to about 11V, a combination of a clamping diode and a 10kΩ resistor may be connected between the relevant terminal point and the +12V supply line; the output pulse should then be taken from the junction of the diode and its resistor (compare 'carry output' in the circuit of Fig. 7).

The voltage dividers formed by R_{10}, R_{20} and R_{30}, and by R_{11}, R_{21} and R_{31} and so forth, have been so dimensioned that large pulses appearing on the +24V supply line when one s.c.s. is switched on will not interfere with any other s.c.s.

Pulse Gate Circuits

The BRY39 lends itself particularly well to use in synchronous gating; that is, in carrying out switching and logic functions that are to be co-ordinated by a train of clock pulses. A synchronous gate responds only when a clock pulse is presented to it concurrently with the required levels at its input terminals. The shape of the output pulse need not depend on that of the input (which may be degraded, as is usually the case in non-synchronous gates); with the aid of the clock pulse, output pulses of well-defined, uniform amplitude and duration can be obtained.

In the gate circuits to be described, input pulses are applied to the collector and clock pulses to the emitter of the s.c.s., output pulses being taken from the anode. Thus negative-going pulses of about 12V, supplied for example by the previously discussed ring counters (Figs. 7 and 10), afford a suitable input (without needing to be inverted), and the output of the gate is itself suitable for driving such a counter.

Simple AND Gate

The operation of the simple gate circuit shown in Fig. 11 may be explained as follows. Negative-going clock pulses reducing the relevant line voltage from ±12V to zero are applied to terminal 1. If, during the presence of such a clock pulse, a negative-going input signal is fed to terminal 2, all conditions are fulfilled for switching on the s.c.s. The resulting anode current flowing through R_2 lowers the potential of terminal 3, giving rise to a negative-going square-wave output pulse that persists until the end of the clock pulse.

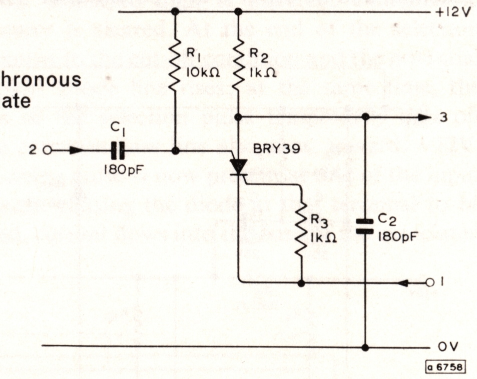


Fig. 11—Synchronous AND gate

Capacitor C_2 limits the feedback introduced by the anode resistor R_2.

AND Gate with Additional Delayed OR Input

The gate circuit shown in Fig. 12 is provided with an additional OR input and incorporates a delay network. If a zero level is applied to any of the diodes D_1, D_2, or D_3, a potential of about 6V appears at the upper end of C_2, so that D_4 is reverse-biased and has no effect. The operation of the circuit is then identical to that of Fig. 11, and provided that a clock pulse is applied to input 1, an input pulse fed to terminal 2 will result in an output pulse.

If, on the other hand, a positive d.c. level of 12V is applied to all diodes D_1, D_2 and D_3, diode D_4 will be forward biased. A negative-going input pulse applied to

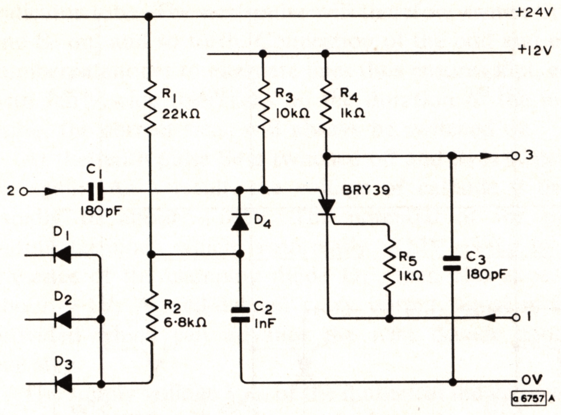

+24V
+12V
R1 22kΩ
R3 10kΩ
R4 1kΩ
BRY39
C1 180pF
D1
D2
D3
D4
R2 6·8kΩ
C2 1nF
R5 1kΩ
C3 180pF
2
3
1
0V
A6757A

Fig. 12—AND gate with additional delayed OR input

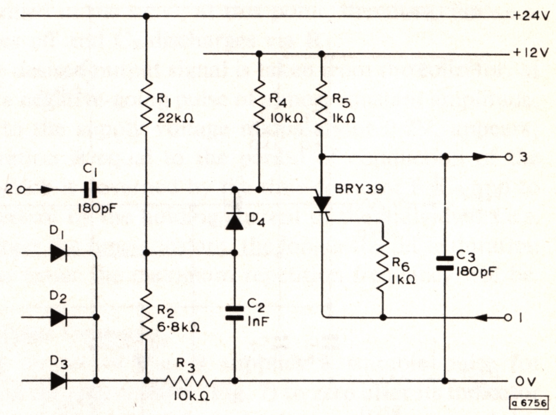

+24V
+12V
R1 22kΩ
R4 10kΩ
R5 1kΩ
BRY39
C1 180pF
D1
D2
D3
D4
R2 6·8kΩ
R3 10kΩ
C2 1nF
R6 1kΩ
C3 180pF
2
3
1
0V
A6756

Fig. 13—AND gate with additional delayed AND input

terminal 2 will therefore be passed by this diode and absorbed by C_2, so that it no longer has any effect.

The network R_2C_2 introduces a delay to ensure that a change of the d.c. level has no effect until the following clock pulse has appeared.

AND Gate with Additional Delayed AND Input

In the circuit of Fig. 13, which is similar to that of Fig. 12, the diodes D_1, D_2 and D_3 are reversed so that the d.c. input forms an AND function. Input pulses fed to terminal 2 will have effect only if all d.c. inputs have zero potential and no input is at a potential of +12V or more.

Control Circuit for Numerical Print-out

Fig. 14 shows a circuit designed for driving a numerical print-out device. Apart from the 'add' and 'non-add' stages, only the first and the last of the ten stages for energising the coils 0 to 9 of the print-out device are shown. For printing-out the complementary digits, as frequently required, the stages 0 to 9 should be connected to the coils 9 to 0 respectively.

The operation of the circuit resembles that of a monostable multivibrator, with S_1, which is normally switched on, governing the period. If one of the switches S_{10} to S_{21} is switched on, a negative-going pulse due to the fall of its anode potential from +12V to about +1V is passed, via C_2 and C_1, to the anode of S_1, causing the latter to be switched off. After its initial drop, however, the anode potential of S_1 rises toward +24V at a rate governed by R_2 and $C_{1,2}$; after a short interval it exceeds the collector potential of +12V, and S_1 again becomes conducting. The negative-going pulse due to the resulting drop in anode potential is then passed, via C_1 and C_2, to the common anode line of S_{10} to S_{21} and causes the s.c.s. which started the cycle to be switched off.

The input circuits for the stages governing coils 0 to 9 are similar to those of the gate circuits discussed earlier. Negative-going clock pulses (or pulses which are derived from and synchronous with them) are fed to their common input terminal. So long as the level of the d.c. input terminal exceeds +12V the corresponding diode (D_{10} to D_{19}) will be conducting, so that these clock pulses have no effect. However, after the d.c. input voltage is made to drop to about zero (1-level) and the corresponding capacitor (for example, C_{20}) is discharged, the diode becomes non-conducting. Owing to the incorporated delay the required s.c.s. is not switched on until the next clock pulse occurs.

Almost the entire current of the switched s.c.s. (about 30mA) then flows into the base of the transistor associated with it; the transistor is thus bottomed and energises the corresponding coil of the print-out device until S_1 returns to the ON state.

The last two stages of the circuit can control the 'add' and 'non-add' coils of the print-out device. After the number to be recorded has been printed out in its entirety, a negative-going pulse fed to the corresponding terminal will directly switch on S_{20} or S_{21} so that the 'add' or 'non-add' coil of the printer is energised.

Diodes D_{20} to D_{31} safeguard the transistors against voltage surges that are apt to be produced across the energising coils when they are switched off.

The circuit can produce energising pulses of up to about 300mA with a duration of 35ms, as required for the less sophisticated types of print-out device. If a faster print-out device is used, requiring energising pulses with a duration of only 1ms, transistors TR_{10} to TR_{21} can be dispensed with and the coils may be connected directly in the s.c.s. anode circuits. And if the energising current required is also smaller (for example 100mA), the circuit can be further simplified by incorporating the coils directly in the s.c.s. collector circuits. In both cases, of course, other appropriate changes must be made in the control circuit.

Numerical Display Unit with Memory

Parallel digits, representing information from a computer or calculator, are often displayed on a bank of numerical indicator tubes, each tube presenting the digit of one decade. A circuit for controlling one such tube in an output display bank is shown in Fig. 15. The s.c.s. associated with each digit acts as a switch and a memory, the digit displayed remaining lit after the information pulse (input signal) that selected it has ceased. The operation of the circuit will be explained with reference to a display bank in which indicator tubes are energised in sequence until the entire numeral to be indicated is displayed.

The indicator tube to be energised is first selected by applying a positive-going pulse to the selection pulse input of the control circuit associated with it. This bottoms transistor TR_1 in the circuit of that tube and drives the anode-emitter voltage of all its associated switches to so low a value that none of them can remain conducting; any previously displayed digit is therefore extinguished and the memory is cleared. At the end of the selection pulse TR_1 returns to the cut-off condition and the potential of the common anode line rises; at the same time, the trailing edge of the selection pulse temporarily cuts off TR_2 and the common base line also rises, toward +12V. If a positive-going pulse is now present at one of the input signal terminals, causing the diode at that terminal to be reverse-biased, current flows into the base of the associated

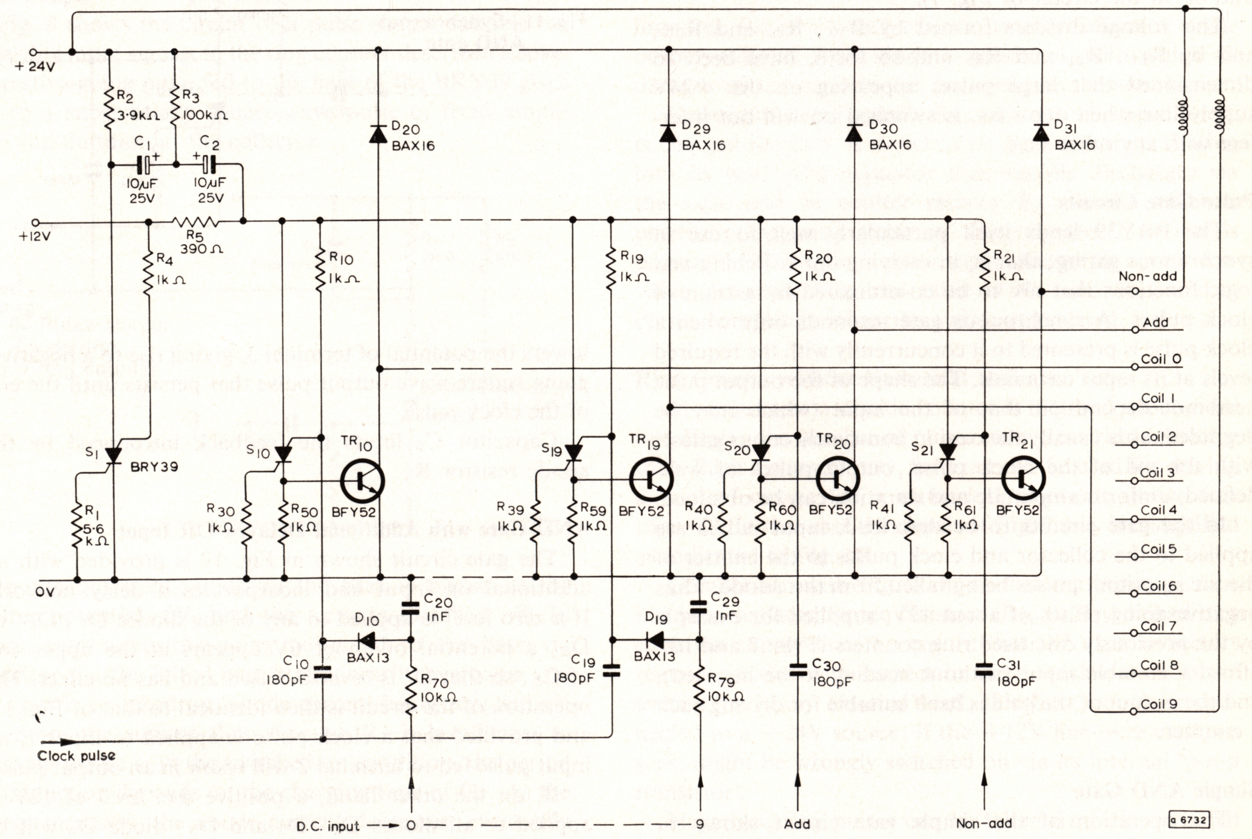

+24V
+12V
R2 3·9kΩ
R3 100kΩ
C1 10µF 25V
C2 10µF 25V
R5 390Ω
R4 1kΩ
R1 5·6kΩ
S1 BRY39
D20 BAX16
D29 BAX16
D30 BAX16
D31 BAX16
R10 1kΩ
R19 1kΩ
R20 1kΩ
R21 1kΩ
S10
S19
S20
S21
TR10
TR19
TR20
TR21
BFY52
R30 1kΩ
R50 1kΩ
R39 1kΩ
R59 1kΩ
R40 1kΩ
R60 1kΩ
R41 1kΩ
R61 1kΩ
0V
D10 BAX13
D19 BAX13
C20 1nF
C29 1nF
C10 180pF
C19 180pF
C30 180pF
C31 180pF
R70 10kΩ
R79 10kΩ
Non-add
Add
Coil 0
Coil 1
Coil 2
Coil 3
Coil 4
Coil 5
Coil 6
Coil 7
Coil 8
Coil 9
Clock pulse
D.C. input 0 — 9
Add
Non-add
A6732

Fig. 14—Control circuit for numerical print-out devices

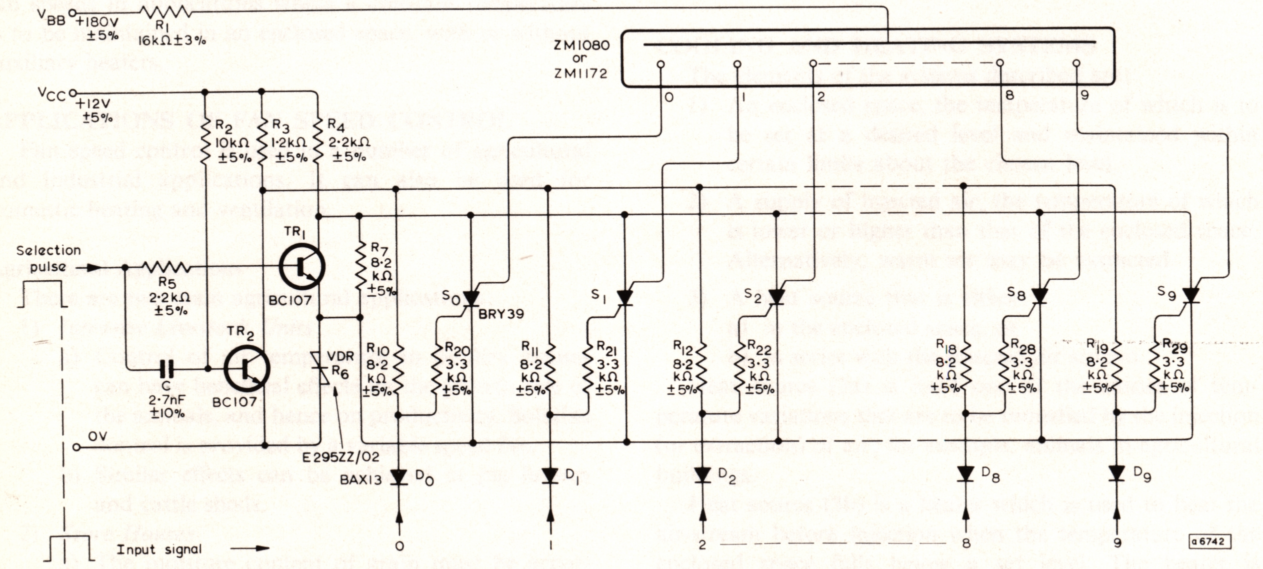

VBB +180V ±5%
R1 16kΩ ±3%
ZM1080 or ZM1172
0
1
2
8
9
VCC +12V ±5%
R2 10kΩ ±5%
R3 1·2kΩ ±5%
R4 2·2kΩ ±5%
TR1 BC107
TR2 BC107
Selection pulse
R5 2·2kΩ ±5%
C 2·7nF ±10%
VDR R6 E295ZZ/02
R7 8·2kΩ ±5%
S0 BRY39
S1
S2
S8
S9
R10 8·2kΩ ±5%
R20 3·3kΩ ±5%
R11 8·2kΩ ±5%
R21 3·3kΩ ±5%
R12 8·2kΩ ±5%
R22 3·3kΩ ±5%
R18 8·2kΩ ±5%
R28 3·3kΩ ±5%
R19 8·2kΩ ±5%
R29 3·3kΩ ±5%
0V
BAX13
D0
D1
D2
D8
D9
Input signal
A6742

Fig. 15—Numerical display with memory

s.c.s. so that it is switched on and the required cathode of the numerical indicator tube is lit. Because of the previously described holding action of the s.c.s., it continues to conduct and the cathode remains lit after the initial input signal has ended.

To ensure that only the required digit is switched on, all diodes must normally be forward biased during the presence of a selection pulse. Except where the bias is momentarily reversed by a positive-going input signal,the currents through R_{10} to R_{19} will then flow through the diodes instead of into the bases of the switches associated with them.

The trailing edge of the selection pulse keeps TR_2 cut off only for a short interval determined by the time constant R_2C. As soon as TR_2 is again bottomed, the common base line returns to a low potential and the voltage drop across the voltage dependent resistor R_6 positively biases the s.c.s. emitters. Any digit input pulse that arrives after the end of the circuit selection pulse therefore has no effect; it cannot cause an s.c.s. to be switched or the indicator tube to change its indication.

This makes it possible to connect similar digit input leads to all indicator tubes in the display bank in common; a digit input pulse applied to the commoned leads will be registered only by that indicator tube whose control circuit has also received a selection pulse. Moreover, the source of the digit input signal is not called upon to supply current to the circuit; on the contrary, the direction of current flow is normally from the control circuit to the signal source (opposite to the direction of the arrows in Fig. 15), and at the terminal to which an input signal is applied it is no more than a very small leakage current. This makes it possible for one low-power transistor to drive a considerable number of commonly connected input terminals if required.

The probe currents of the unlit cathodes do not affect the operation of the circuit. Owing to the s.c.s. emitters being positively biased by R_6, the probe currents are conducted via the collector, the base, and the base resistors of each s.c.s. and thence via the bottomed transistor TR_2 to earth without causing the base-emitter junction of any s.c.s. to become forward biased. In this way the collector voltages are prevented from oscillating.

To extinguish the indicator tube, it is sufficient to apply a positive-going pulse to the selection pulse input while all digit inputs are at their (normal) low potential; this will switch off any conducting s.c.s. and extinguish the indicator tube cathode associated with it.

The 180V supply V_{BB} and the 12V supply V_{CC} should be constant within ±5%. The high level of both the selection pulse and the digit input signal may range from ±4V to ±25V; the recommended value is +6V. The low level may range from −1V to +0·2V, zero being recommended. The duration of the selection pulse should not be less than 6μs and that of the digit input signal not less than 5μs; the input signal should be applied before the end of the selection pulse.

Thyristor Control of Fan Cooling and Heating Systems

D. HUMPHRIES and J. LAVALLEE
Mullard Central Application Laboratory

Fans, driven by a.c. induction motors and used in conjunction with heaters, may be used to control the air temperature in buildings. Automatic maintenance of the temperature within close limits may be provided by controlling the fan speed by means of variable slip speed control. In the systems described, a thermistor senses the air temperature, and a simple transistor circuit varies the triggering angle of the thyristors in the motor supply, thus varying the voltage applied to the motor and controlling the motor speed.

To increase the flexibility of the basic system so that it can be used in a variety of applications, supplementary circuits to provide heater switching, fan speed control within maximum and minimum limits, and other facilities, are described.

INTRODUCTION

The speed of an a.c. induction motor may be varied from zero to near synchronous speed by changing the supply voltage. This method of speed control may be used on a high-resistance rotor induction motor with any type of load or on a low-resistance rotor induction motor with non-linear (square or cube law) type loads such as fans or centrifugal pumps.

This article studies the characteristics of both high-resistance and low-resistance rotor induction motors with particular reference to fan loads, and it describes circuits for controlling the speed of a fan by means of thyristors.

The practical circuits have been designed to control fan speeds in applications where a constant temperature is to be maintained in an enclosed space, with or without auxiliary heaters.

APPLICATIONS OF FAN SPEED CONTROL

Fan speed control is used in a number of agricultural and industrial applications. It can also be used for domestic heating and ventilation.

Agricultural Applications

There are two main agricultural applications:

1) *Intensive Livestock Units*
    a) Control of air temperature in poultry houses can have beneficial effects on the growth rate of the animals, and hence on productivity. Suitable control is provided by a variable speed fan.
    b) Similar effects can be achieved in pig houses and cattle sheds.
2) *Store Houses*
    a) The moisture content of grain must be accurately controlled to prevent disease, rotting, or germination during storage. A controlled-speed fan injecting heated air can provide the required humidity control for the preparation of grain for storage.
    b) Storage of grain or other products, such as fruit, requires the maintenance of a steady predetermined temperature throughout the storage period. The required temperature may be fairly low, although not so low that refrigeration is necessary. A controlled-speed fan will serve this purpose.

Industrial Applications

1) Any application in which automatic or manually controlled ventilation by air injection or extraction is required, can be carried out satisfactorily by the use of a controlled-speed fan.
2) A controlled-speed fan can be used to control the temperature of an oil-fired oven or kiln.
3) Air conditioning of work-spaces requires an automatically controlled-speed fan and a heater.

Domestic Heating

In fully automatic heating and ventilation systems for domestic use, the speed of the fan is automatically increased when the room temperature rises above a set level, and also increases below a set level in conjunction with an electric, gas, or oil heater.

COOLING AND HEATING SYSTEMS

The elements of the systems described are:

1) An enclosed space, the temperature of which is to be set at a desired level and maintained within certain limits about the chosen level.
2) A supply of injected air, the temperature of which is lower or higher than that of the enclosed space. Alternatively, warm air may be extracted.
3) A heat source that is either:
    a) in the enclosed space, or
    b) in series with the injected air stream.

Heat source (3a) is itself one of the causes of temperature variations that are to be remedied by the injection (or extraction) of air; for example, animals in agricultural buildings.

Heat source (3b) is a heater which is used to heat the air-stream before injection when the temperature of the enclosed space falls below a set level. The heater is switched either to be on or off.

The temperature of the enclosed space will vary because of heat generation by the occupants (as in 3a) and variation of the atmospheric temperature (or other ambient conditions) outside the walls. Good thermal design will reduce the effects of ambient temperature changes, but not eliminate them completely. The heating effect of the occupants will always be present.

If the room temperature tends to rise above the maximum level, cool air can be injected by a fan. If the temperature falls below a minimum set level, the fan can inject heated air. Between these two set levels both heater and fan would be off.

CONTROL REQUIREMENTS

There are several possible controls, some of which may be obligatory in a practical system, and some of which may be regarded as refinements.

Automatic Control of Fan Speed

It is desirable that an automatic system, controlled by a temperature sensor, adjusts the rate at which the fan either:

1) injects cool air (or extracts heated air) to reduce a temperature that is too high, or
2) injects heated air to increase a temperature that is too low.

In case (1), the higher the temperature the higher the fan speed. In case (2), the lower the temperature the higher the fan speed (but care must be taken to ensure that the air taken in by the fan is not so cold that it will swamp the effect of the heater).

Manual Control of Fan Speed

It is sometimes necessary to have a simple manual control independent of the temperature sensing device.

Heater Switching

Automatic heater switching is necessary to save power and to prevent overheating of the enclosed space. If the heater were permanently on, the space might overheat beyond the capacity of the fan to keep the temperature down even at maximum fan speed.

Speed Limits

Limiting the minimum speed of the fan may be necessary to prevent overheating of the motor if it is not designed to run at low speeds or low airflow. It may also be desirable to have a continuous supply of air for adequate ventilation, independently of the airstream controlled by the temperature sensor.

Some applications may require a control to limit the maximum speed of the fan so that the occupants of the room are not subjected to discomfort.

Choice of Set Temperature

If the room temperature is to be maintained at one level on some occasions and at another level on others, a means of adjusting the system to operate at any chosen temperature will be required.

INDUCTION MOTOR CHARACTERISTICS

Before a fan control circuit can be designed it is necessary to study the characteristics of both low-resistance and high-resistance rotor induction motors when used on linear and non-linear loads.*

Figs. 1 and 2 show the torque/slip speed characteristics for low-resistance and high-resistance induction motors. If the low-resistance motor operating at constant torque at variable voltage is considered first, then it can be seen that at normal supply voltage V_1 the load/torque line cuts the motor characteristic at A (Fig. 1) giving maximum speed at low values of slip.

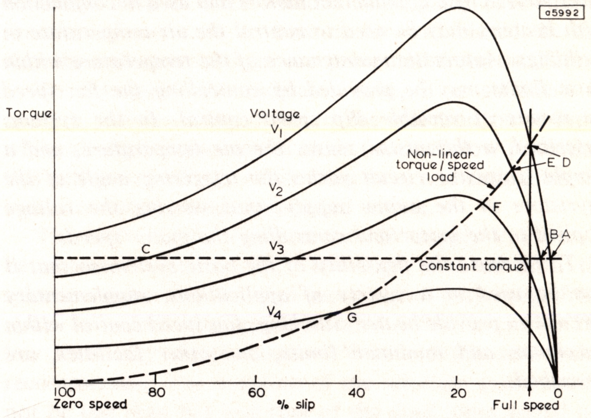


Fig. 1—Torque/slip characteristics for low-resistance rotor induction motor

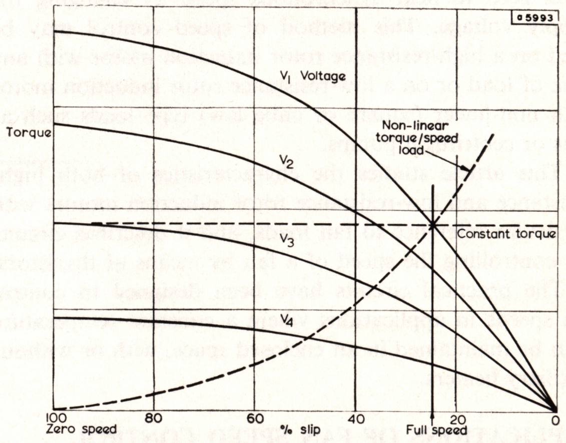


Fig. 2—Torque/slip characteristics for high-resistance rotor induction motor

A constant torque load will always cut the motor characteristic at two points. These two points, shown as B and C with a supply voltage V_2, will give two operating conditions; at point C unstable operation results whilst at B the range of speed as a function of voltage is smaller.

With the non-linear load characteristics, also shown in Fig. 1, the motor torque/speed load line cuts each voltage characteristic only once, at points D, E, F, and G, all of which are stable points of operation.

It can be seen in Fig. 2 that each voltage characteristic for the high-resistance motor is cut by the load characteristic only once, be it for a constant torque load or a non-linear load. The efficiency and speed regulation of such a system of speed control applied to a high-resistance motor is poor, and the system is seldom used for other than fan control.

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*The characteristics of induction motors and their efficiencies are dealt with more fully in Ref. 1.

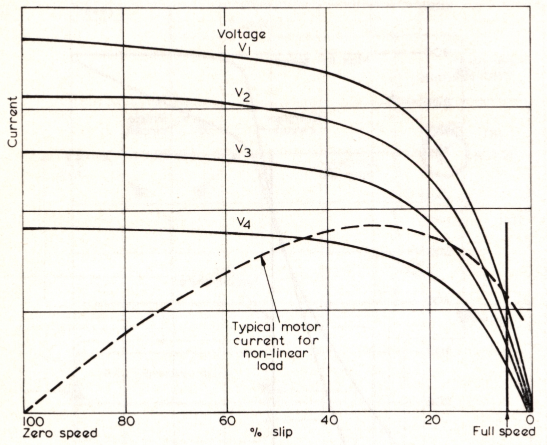

Fig. 3—Current/slip characteristics for low-resistance rotor induction motor

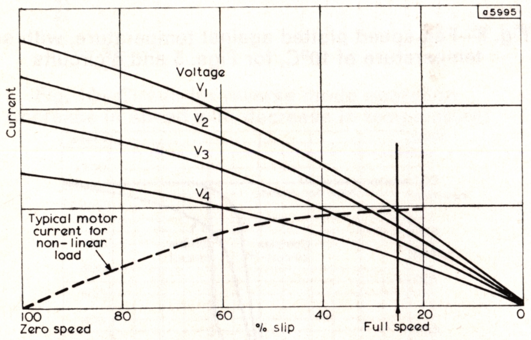

Fig. 4—Current/slip characteristics for high-resistance rotor induction motor

Figs. 3 and 4 show the current/slip characteristics for low-resistance and high-resistance induction motors, also the motor currents which would be obtained if the load were a fan with a torque/speed characteristic as shown in Figs. 1 and 2.

The starting current may be up to three times the normal running current, depending upon the position of the operating point on the motor characteristic. Information on starting currents must be obtained from the motor manufacturer before the thyristor stack is selected.

MOTOR POWER CIRCUITS

The same motor circuit is used in all systems. The a.c. voltage to the motor is controlled by a conventional single-phase thyristor a.c. controller. Allowance must be made for the starting current surges when selecting the size of the thyristor to be used in the a.c. controller.

If a high-resistance motor is used, this type of speed control may be used with almost any type of load. But since motor losses are high at low speeds, external motor cooling may be necessary for any but the smallest motor.

PRACTICAL FAN COOLING CIRCUITS

A number of practical circuits have been designed, ranging from a simple circuit which incorporates manual control of fan speed, to a circuit which incorporates all the features discussed in this article.

Automatic Control

Figs. 5 and 6 show two circuits for automatic fan speed control; Fig. 6 is a circuit providing considerably greater sensitivity. Both systems include the MY5001 module blocking oscillator circuit shown in Fig. 7.

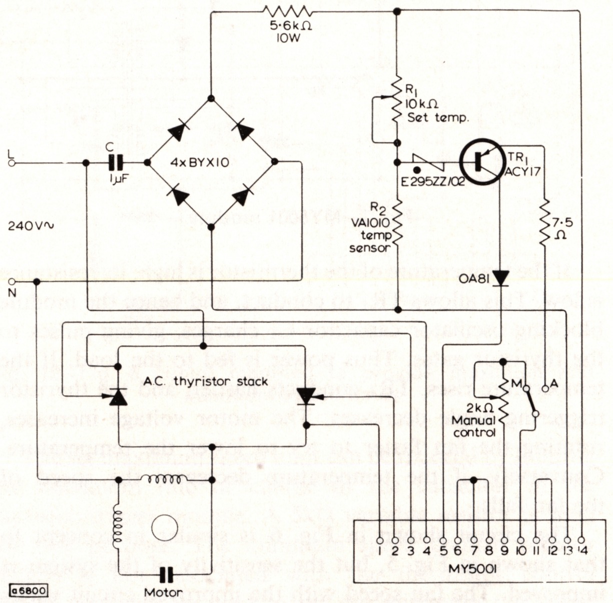

Fig. 5—Fan speed control

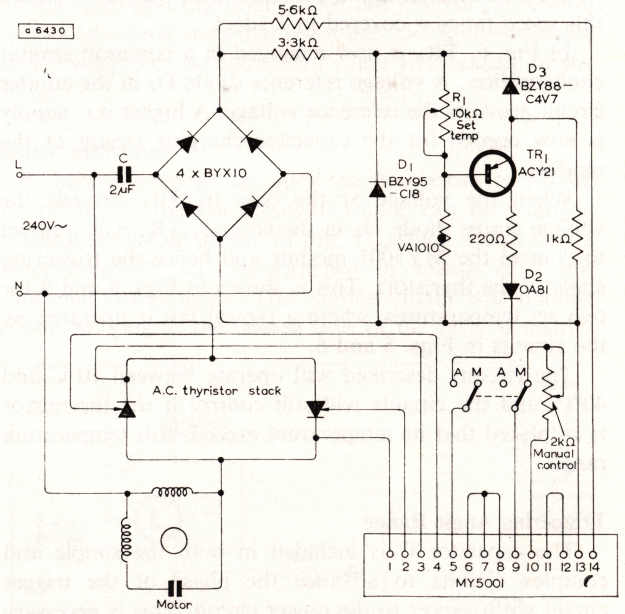

Fig. 6—Complex fan speed control

The transistor TR$_1$ in the temperature control circuit of Fig. 5 controls the charging rate of the capacitor C_1 in the module circuit of Fig. 7. The TR$_1$ base current is varied by either the set temperature control R_1 or the temperature sensor R_2. The asymmetrical v.d.r. acts as a 1·3V voltage reference diode which prevents TR$_1$ from conducting until the voltage set by R_1 and R_2 exceeds this level.

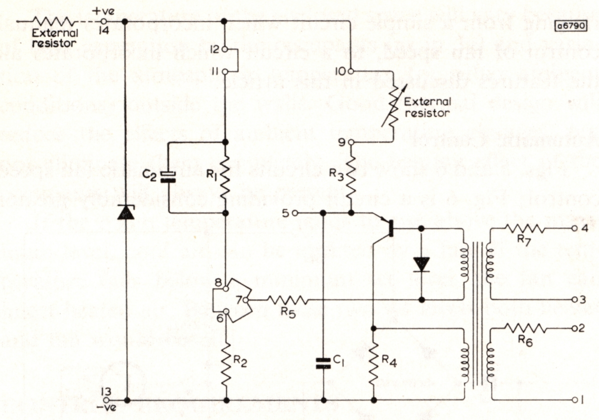
e6790
External resistor
+ve 14
12
11
10
External resistor
9
C2
R1
R3
5
R7
4
8
7
R5
6
3
R6
2
R2
C1
R4
13 −ve
1

Fig. 7—MY5001 module

If the temperature of the thermistor is high, its resistance is low. This allows TR_1 to conduct, and hence the module blocking oscillator capacitor C_1 charges, giving pulses to the thyristor gates. Thus power is fed to the load. If the temperature rises, TR_1 conducts harder, and the thyristor triggering angle decreases. The motor voltage increases, rotating the fan faster to try to lower the temperature. Conversely, if the temperature decreases the speed of the fan falls.

The circuit shown in Fig. 6 is similar in concept to that shown in Fig. 5, but the sensitivity of the system is improved. The fan speed with the improved circuit varies from zero to maximum in 2·5degC; with the Fig. 5 circuit this speed range is covered in 7·5degC.

In Fig. 6, TR_1 is now arranged in a common emitter configuration. A voltage reference diode D_3 in the emitter circuit provides the reference voltage. A higher d.c. supply is now needed for the capacitor charging circuit of the module.

When the voltage at the base of TR_1 exceeds the voltage across diode D_3 in the emitter, TR_1 will conduct to control the MY5001 module and hence the triggering angle of the thyristors. This is shown in Figs. 8 and 9 for two set temperatures, where a typical fan is operated by the circuits in Figs. 5 and 6.

The circuits described will operate between 10°C and 40°C, and the circuits will still control if the thermistor is so placed that its temperature exceeds this temperature range.

Triggering Angle Range

The capacitor C is included in both the simple and complex circuits to advance the phase of the trigger circuit with respect to the power circuit. This is necessary because the range of triggering angle provided by a blocking oscillator trigger circuit, such as the MY5001, is restricted to about 110° (between 50° and 160°). For fan speed control the supply series capacitor C advances the triggering angle from approximately 20° to 130°.

Manual Control

Figs. 5 and 6 show how the circuits can be switched from automatic control to manual control. If automatic control is not required, only the 2kΩ variable resistor need be used. Transistor TR_1 and its associated components can be omitted; but the 5·6kΩ resistor in the supply line to terminal 14 is retained.

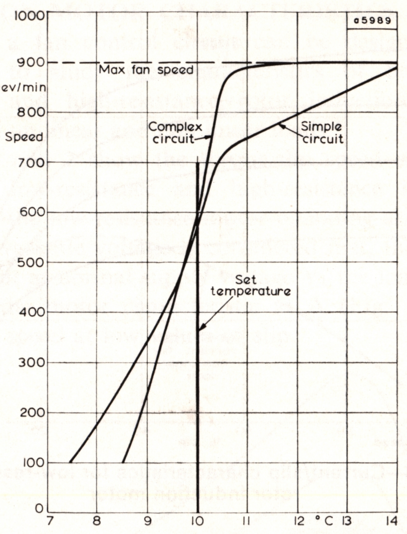

Fig. 8—Fan speed plotted against temperature, with set temperature of 10°C, for Figs. 5 and 6 circuits

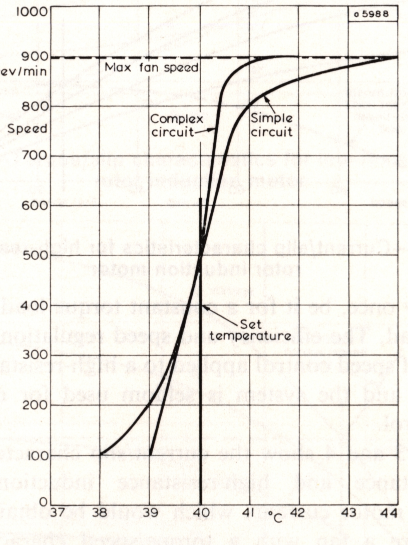

Fig. 9—Fan speed plotted against temperature, with set temperature of 40°C, for Figs. 5 and 6 circuits

ADDITIONAL FACILITIES

It is relatively simple to add modifications to the above circuits to fulfil other possible requirements of a fan cooling and heating system.

Reverse Mode Operation

The circuits shown in Figs. 5 and 6 provide an increased fan speed when the room temperature rises. For reverse mode operation the circuit shown in Fig. 10 will operate the fan from zero to maximum speed, with a heater switched on, when the temperature of the building falls below a point determined by the set temperature control. The characteristic of the circuit is shown in Fig. 11 where a temperature change of 2·5degC is shown to have taken the fan through its complete speed range.

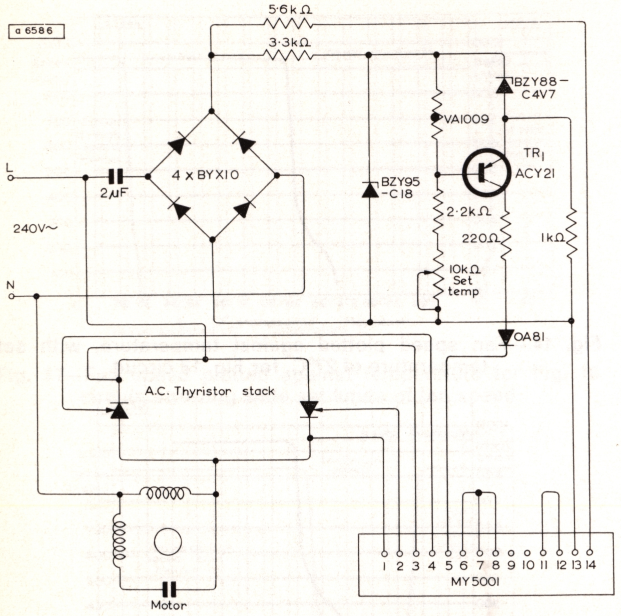
e6586
5·6kΩ
3·3kΩ
BZY88−C4V7
VA1009
L
2μF
4 x BYX10
TR1
ACY21
BZY95−C18
240V~
2·2kΩ
220Ω
1kΩ
10kΩ
Set temp
N
OA81
A.C. Thyristor stack
Motor
1 2 3 4 5 6 7 8 9 10 11 12 13 14
MY5001

Fig. 10—Circuit for reverse mode operation (increase in speed with decrease in temperature)

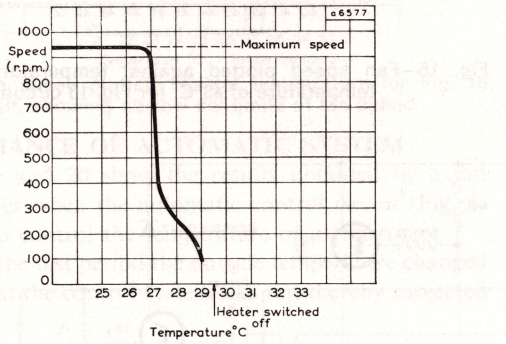

Fig. 11—Fan speed plotted against temperature for Fig. 6 circuit modified for reverse mode operation

Maximum and Minimum Speed Controls

Maximum and minimum speed controls are provided by the modifications shown in Fig. 12. They can be used with all the circuits described.

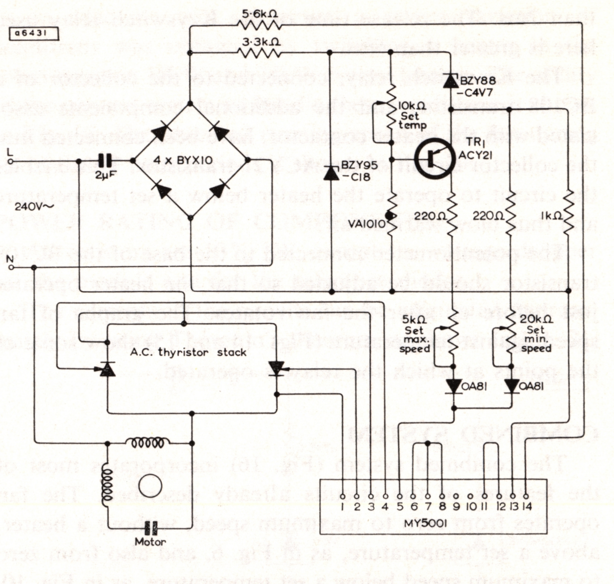
e6431
5·6kΩ
3·3kΩ
BZY88−C4V7
10kΩ
Set temp
TR1
ACY21
L
2μF
4 x BYX10
BZY95−C18
240V~
VA1010
220Ω
220Ω
1kΩ
N
5kΩ
Set max. speed
20kΩ
Set min. speed
A.C. thyristor stack
OA81
OA81
Motor
1 2 3 4 5 6 7 8 9 10 11 12 13 14
MY5001

Fig. 12—Fig. 6 circuit modified to provide maximum and minimum speed limits

The set maximum speed limit can be reduced by limiting the maximum rate of charge of the capacitor in the thyristor trigger module. A 5kΩ variable resistor is used for this purpose. The minimum speed control resistor (20kΩ) is not associated with the thermistor control circuit, and can be used to set the minimum fan speed between zero and maximum. This last control can ensure a minimum speed such that the losses in a high-resistance motor would not be enough to cause overheating of the motor.

Heater Switching

Switching a heater on after the fan begins to rotate, and off before the fan ceases to rotate, can be arranged by using the circuit shown in Fig. 13, which shows how a heater contactor can be switched by means of a few additional components. This simple circuit will operate reliably so long as the release time of the relay is greater

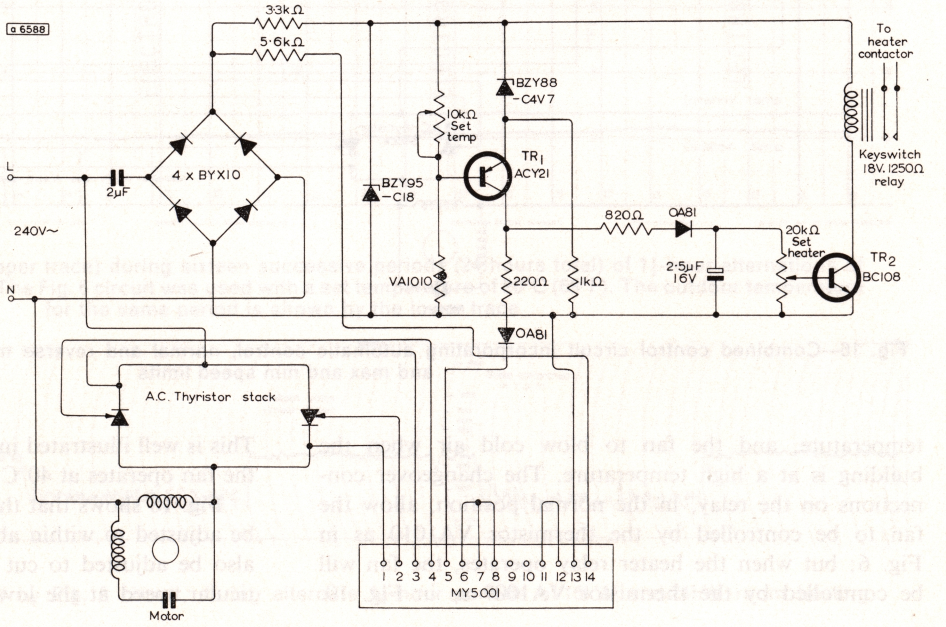
e6588
3·3kΩ
5·6kΩ
To heater contactor
BZY88−C4V7
10kΩ
Set temp
TR1
ACY21
L
2μF
4 x BYX10
BZY95−C18
Keyswitch 18V, 1250Ω relay
240V~
820Ω
OA81
20kΩ
Set heater
2·5μF 16V
TR2
BC108
N
VA1010
220Ω
1kΩ
OA81
A.C. Thyristor stack
1 2 3 4 5 6 7 8 9 10 11 12 13 14
MY5001
Motor

Fig. 13—Circuit enabling heater to be switched on or off when fan starts to rotate

than 2ms. The release time of the Keyswitch relay used here is greater than 6ms.

The Keyswitch relay, connected to the collector of a BC108 transistor, and the additional components associated with the heater contactor, have been connected into the collector circuit of the ACY21 transistor. This enables the circuit to operate the heater below a set temperature and thus blow warmed air.

The potentiometer connected to the base of the BC108 transistor should be adjusted so that the heater operates just before or after the fan rotates. The graphs of fan speed against temperature (Figs. 14 and 15) show some of the points at which the relay is operated.

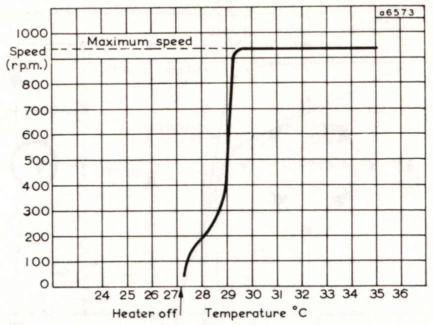

Fig. 14—Fan speed plotted against temperature, with set temperature of 27°C, for Fig. 13 circuit

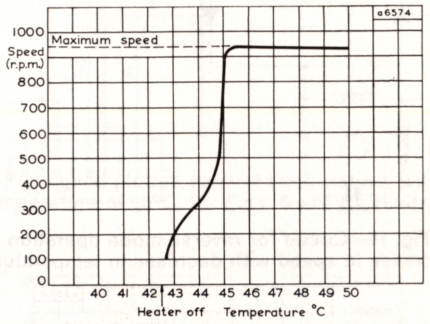

Fig. 15—Fan speed plotted against temperature, with set temperature of 43°C, for Fig. 13 circuit

COMBINED SYSTEM

The combined system (Fig. 16) incorporates most of the features of the circuits already described. The fan operates from zero to maximum speed, without a heater, above a set temperature, as in Fig. 6, and also from zero to maximum speed below a set temperature, as in Fig. 10. Heater switching facilities enable the temperature of the room to be raised.

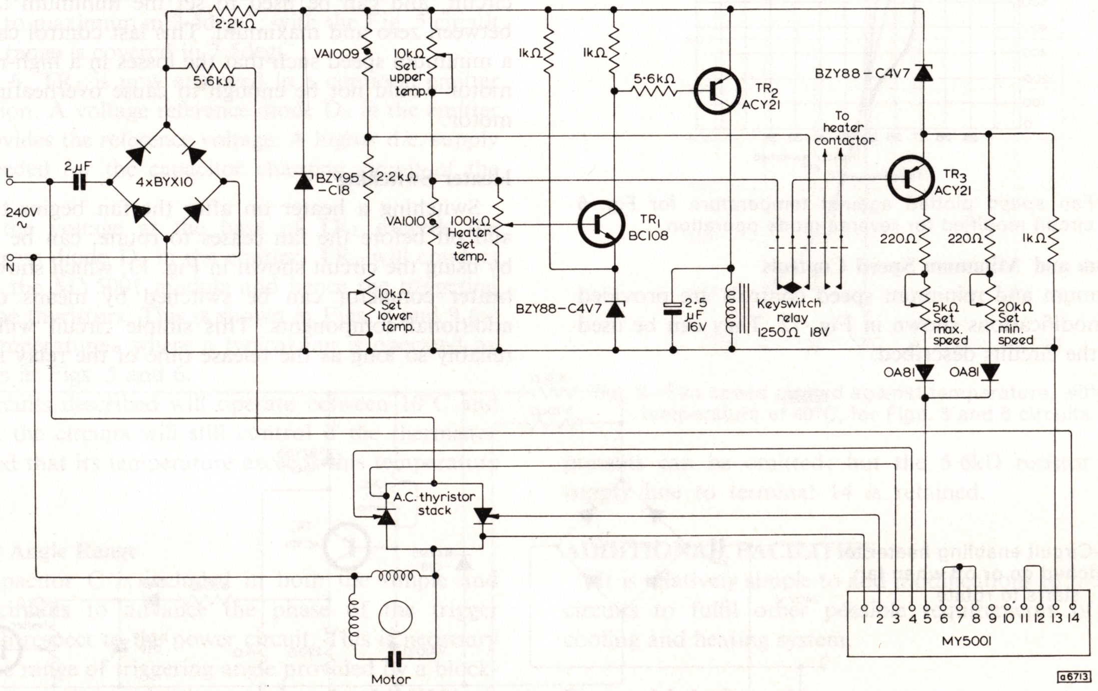
2·2kΩ
5·6kΩ
VA1009
10kΩ Set upper temp.
1kΩ
1kΩ
5·6kΩ
TR2 ACY21
BZY88–C4V7
To heater contactor
L
2µF
4×BYX10
240V ~
N
BZY95 –C18
2·2kΩ
VA1010
100kΩ Heater set temp.
TR1 BC108
TR3 ACY21
220Ω
220Ω
1kΩ
10kΩ Set lower temp.
BZY88–C4V7
2·5 µF 16V
Keyswitch relay 1250Ω 18V
5kΩ Set max. speed
20kΩ Set min. speed
OA81
OA81
A.C. thyristor stack
Motor
1 2 3 4 5 6 7 8 9 10 11 12 13 14
MY5001
a6713

Fig. 16—Combined control circuit incorporating automatic control, normal and reverse mode operation, heater switching, and max and min speed limits

An additional transistor TR₂ is required to switch the heater relay, as it is necessary to operate the heater control directly from the thermistor VA1010. This enables the heater to be switched on when the building is at a low temperature, and the fan to blow cold air when the building is at a high temperature. The changeover connections on the relay, in the normal position, allow the fan to be controlled by the thermistor VA1010 as in Fig. 6; but when the heater relay operates, the fan will be controlled by the thermistor VA1009 as in Fig. 10. This is well illustrated in Fig. 17 where it can be seen that the fan operates at 40°C and 6°C, and the heater at 10°C.

Fig. 18 shows that the cold and hot air conditions can be adjusted to within about 1·5degC, and the heater can also be adjusted to cut off when the fan reaches a particular speed at the lower temperature setting.

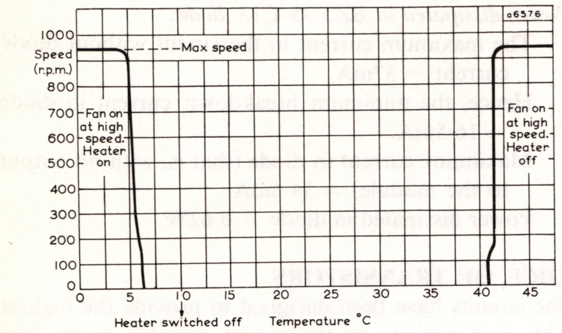

Fig. 17—Fan speed plotted against temperature for Fig. 16 circuit, showing wide set limits of fan speed

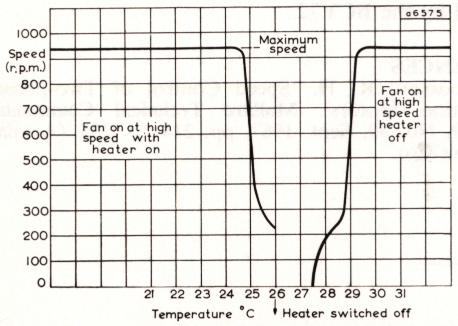

Fig. 18—Fan speed plotted against temperature for Fig. 16 circuit, showing narrow set limits of fan speed

PERFORMANCE OF AUTOMATIC SYSTEM

Figs. 19 and 20 show the results obtained by a fan manufacturer when the automatic control circuit (Fig. 6) was used to control the temperature of a test room.

During the test period the outside temperature changed little, so that the control system was not thereby subjected to an adequate trial. However, a severe variation of conditions was obtained by switching a heater in the room between 15kW and 24kW every 1½ hours. The ability of the control system to handle these conditions is shown in Fig. 19. The observed running speed of the fan during six of the 1½ hour periods is shown in Fig. 20.

POWER RATING OF COMPONENTS

All resistors are 10% ¼W, except the voltage dropper for the module and for the reference diodes.

The currents in the circuits can be calculated approximately by using Thévenin's theorem, as shown in Fig. 21,

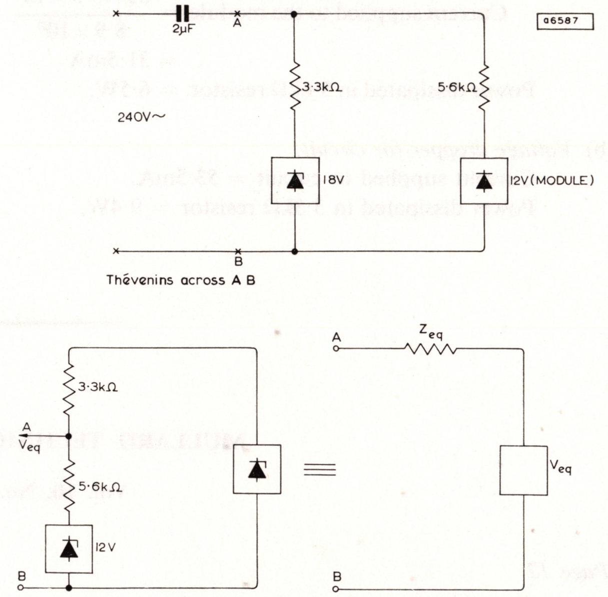
a6587
2µF
A
3·3kΩ
5·6kΩ
240V~
18V
12V (MODULE)
B
Thévenins across A B
A
Zeq
3·3kΩ
A
Veq
5·6kΩ
12V
B
B
Veq

Fig. 21—Approximate equivalent circuit of fan speed control

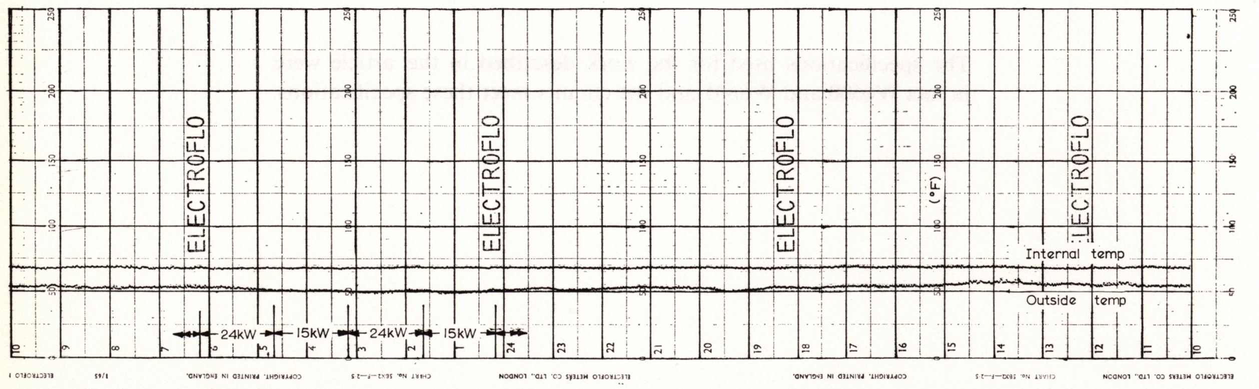

Fig. 19—Room temperature (upper trace) during sixteen successive periods (24 hours total) of 1½-hour alternations of 15kW and 24kW room heating. The Fig. 6 circuit was used with a set temperature of 20°C (68°F). The outdoor temperature for the same period is shown by the lower trace

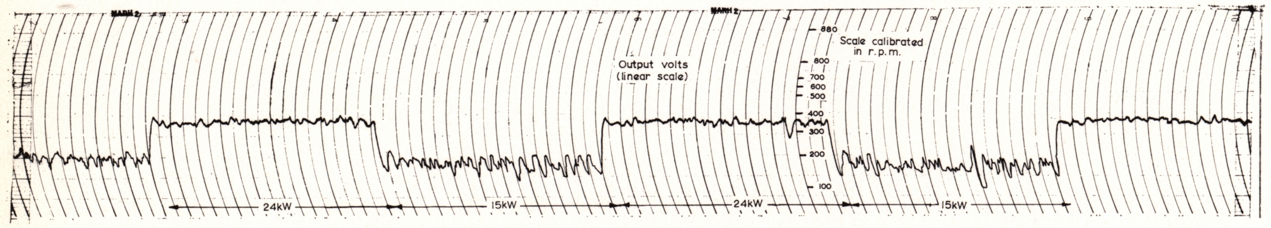

Fig. 20—Fan speed, controlled by Fig. 6 circuit, during alternate 1½-hour periods of 15kW and 24kW room heating

by the following:

$$V_{eq} = 12V + \frac{6V \times 5 \cdot 6 \times 10^3}{8 \cdot 9 \times 10^3} = 16V.$$

$$Z_{eq} = \frac{3 \cdot 3 \times 5 \cdot 6 \times 10^6}{8 \cdot 9 \times 10^3} = 2 \cdot 08\Omega.$$

$2\mu F$ capacitor reactance $= 1 \cdot 6k\Omega$

$$\text{Hence capacitor current} = \frac{240 - 16}{2 \cdot 08 \times 10^6 - j1 \cdot 6 \times 10^3} = 85mA \angle 38^\circ.$$

a) *Voltage dropper for module:*

$$\text{Current supplied to the module} = \frac{85 \times 3 \cdot 3 \times 10^3}{8 \cdot 9 \times 10^3} = 31 \cdot 5mA$$

Power dissipated in $5 \cdot 6k\Omega$ resistor $= 6 \cdot 5W$.

b) *Voltage dropper for circuit:*

Current supplied to circuit $= 53 \cdot 5mA$.

Power dissipated in $3 \cdot 3k\Omega$ resistor $= 9 \cdot 4W$.

c) *Power dissipated in BZY95–C18 diode:*

The maximum current in the circuit without diode current $= 37mA$.

Hence, the minimum breakdown current in diode $= 16 \cdot 5mA$.

Maximum current in diode (that is, with no output to the module) $= 34 \cdot 5mA$.

Power dissipated in diode $= 0 \cdot 62W$.

CHOICE OF TRANSISTORS

The circuits have been designed to provide the highest possible performance at the lowest possible price. The ACY21 germanium transistor achieves this. If, however, it is wished to use silicon transistors, the ACY21 can be replaced by the BCY72.

REFERENCES

1. Williamson, K. H. 'Speed Control of Two-phase A.C. Induction Motors'. **Mullard Technical Communications,** Vol. 9, No. 89, Sept. 1967, pp. 214 to 238. (Available as Reprint Co).

MULLARD TECHNICAL COMMUNICATIONS

Vol. 10, No. 91, January 1968

Page 12

Reference 1 should read
'Private Land Mobile Radio Services', G.P.O. Specifications W6600 and W6601.

Page 28

Reference 2 should read
'Private Land Mobile Radio Services' G.P.O. Specifications W6600 and W6601.

The specifications used for the work described in the article were in fact W6600 and W6601 and the circuits meet these specifications.